



CMS Pixel Front-End Controller

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Basic requirements

CMS Front-End Controller (FEC) main functions (as per CMS documents):

- **Generate timing and trigger signals for the front-end event pipeline delays and event buffering logic**
- **Generate necessary initialization and setup commands for the front-ends**
- **Provide necessary means for monitoring and remote diagnostics of the front-ends**



Basic assumptions

- Use CMS “standard” opto-electrical hardware (DTRx4, TTCrq) for external communications
- Use 9U VME form factor that allows sufficient number (8..12) of FEC channels per board
- Provide a compatible interface to a networked VME master for communications with DCS and RCMS
- Use a hardware controller and a large memory for each FEC channel to guarantee a minimum “refreshing” rate of ROC/TBM settings
- Use private gap and private orbit TTC signals (B-Go commands) to synchronize “refreshing” operations to the beam timing
- Implement return clock signal for reliable data reception



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Benefits:

- Reliable (hardware based) synchronization to the accelerator timing (gap, orbit)
- No commands are required from the VME master during “refreshing” operations
- High channel density per VME card (12) allows to use one FEC crate for Pixel detector

Drawbacks:

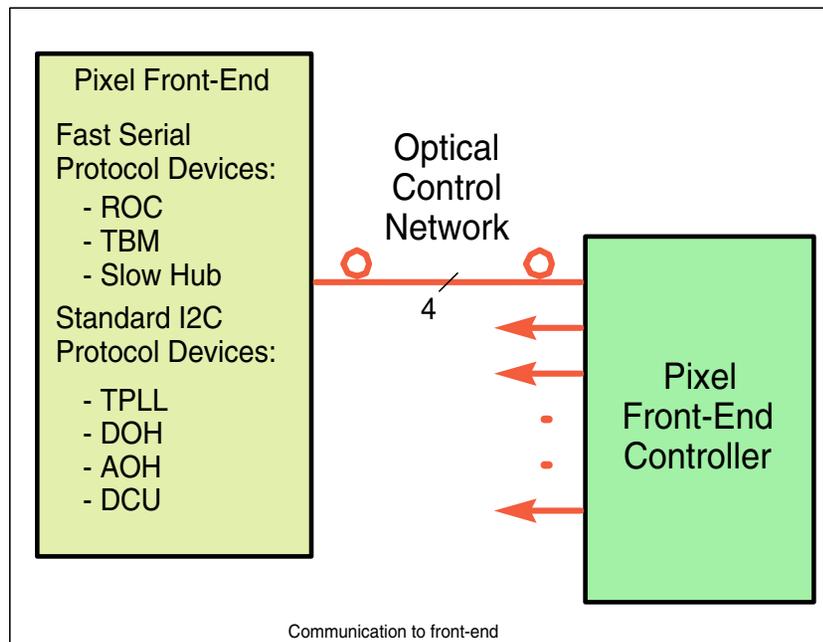
- Requires a Slow Hub chip compatible with fast serial protocol (could be designed by Fermilab EED ASIC Projects group in 4..5 months)



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Communication to the front-ends

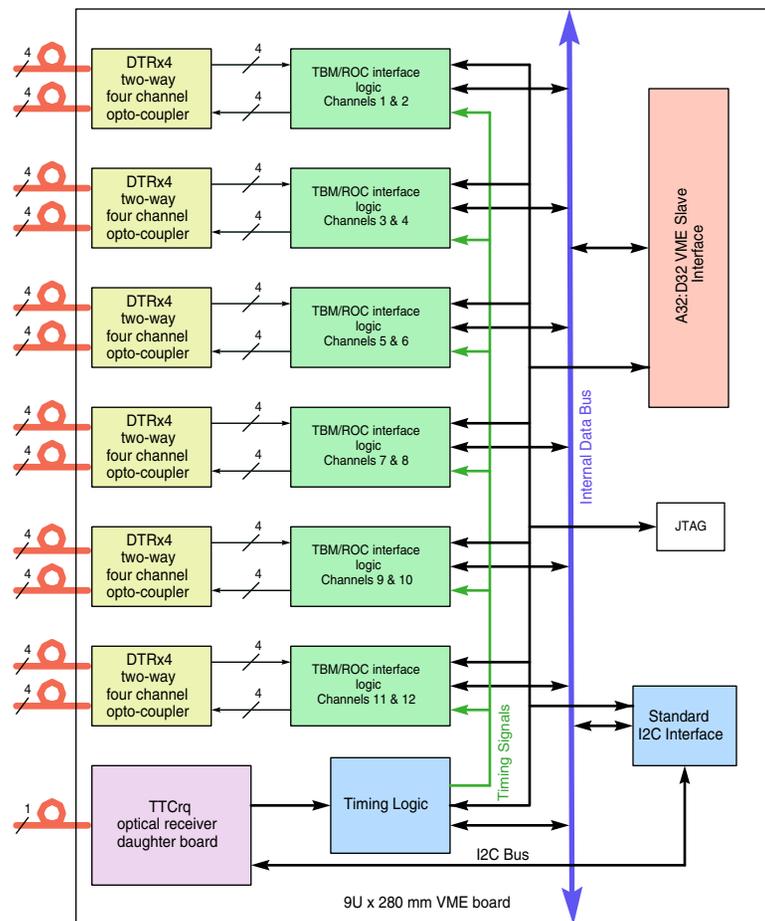
- Fast serial protocol using data and clock lines (I2C based) @ 40 MHz with each 4th data bit inverted and added as a 5th bit – requires design of a compatible Slow Hub chip





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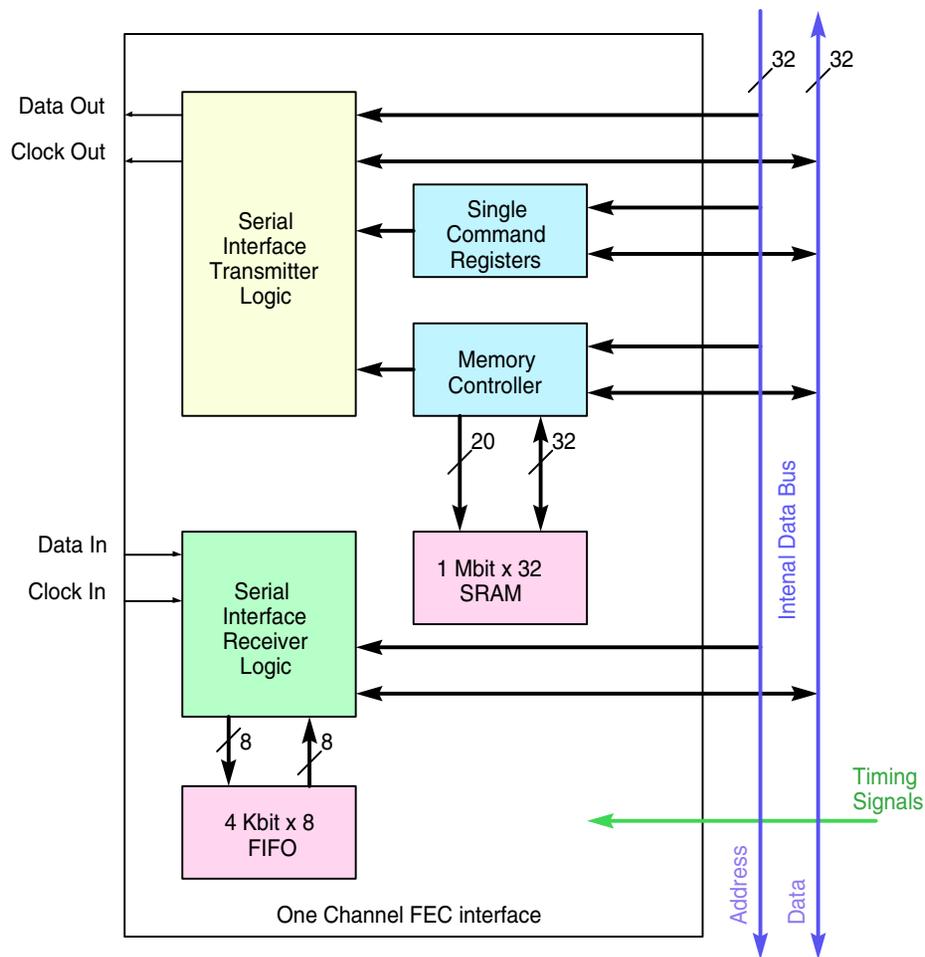
FEC block-diagram





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One channel block-diagram





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Summary

- **A preliminary specification of the Pixel FEC has been finalized in February 2004**

(see full document at the following URL:

http://ppd.fnal.gov/experiments/forward_pixel/Electronics/FEC_spec_01.pdf)

- **Resources are currently available at Fermilab**
- **First prototype may be available in 10..12 months after the final spec is frozen**