



U S C M S
The Compact Muon Solenoid Collaboration

CMS Pixel Chip PSI46 - on wafer testing results -



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Overview

- This presentation is a summary of a testing procedure, equipment used and content of a report file for PSI46 wafer testing
- We have tested two wafers, each with 66 recticles. Each recticle comprises four PSI46 chip versions, labeled A, B, C and C-T

Wafer Test Station (1)

Equipment:

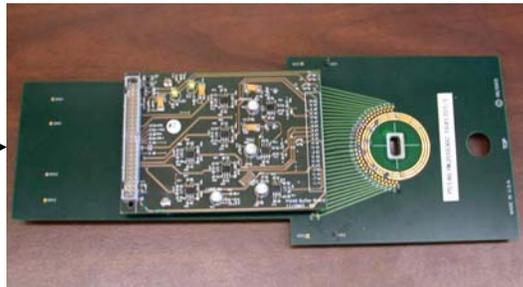
- Cascade/Alessi 6171 semi-automatic 8 inch chuck probe station (1)
- EED ASIC Test System (2)
- Application specific ASIC Interface Board and PSI46 Buffer Board (4)
- Custom designed PSI46 probe card (3)



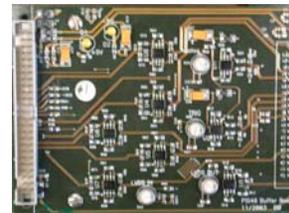
1



2



3

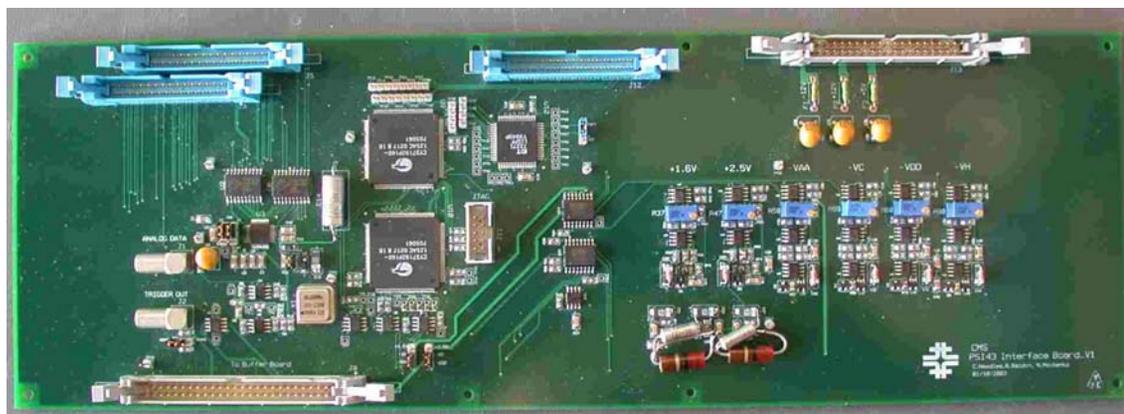


4

Wafer Test Station (2)

ASIC Interface Board features:

- Two programmable power supplies with shutdown
- DC voltage (five values) and current (two values) measurements
- Serial command interface with two modes of operations:
 - Single command
 - FIFO command stream
- Timing generator with programmable Calibrate and Trigger pulses
- 12 bit, 80 MHz ADC for analog data sampling
- Independently selectable clock frequencies for serial command interface and timing generator (40, 20, 10 and 5 MHz)
- Programmable PSI46 serial interface address



PSI46 Test file structure

The main steps during a chip test are:

- Set interface board I2C address (adrs1), calibrate pulse number (ncal), trigger pulse number (ntrig), token delay (tokendel), PSI46 and I2C frequency (freq) and I2C clock to 'external'. These parameters are not changed during test.
- Load interface board FIFOs with
 - a) PSI46 DAC settings (suggested values from PSI) and
 - b) program data for all pixels with mask bit=1 and trim=8 (0 to 15)
- Set programmable power supply ON (psdig=2V, psana=1.5V) and do chip reset
- Read power supply currents and voltages (first time)
- Start FIFO stream download to PSI46
- Read power supply currents and voltages (second time)
- Issue a single sequence, do timing reset and do clear calibration (clears all pixels data)
- Start a pixel cycle, which measures two consecutive rows (same column) at a time. Repeat this 40 times (to cover all 80 rows in a column) then go to next column and repeat cycle. In each cycle we use clr_cal command to clear all pixels, then cal_pix command to enable two new rows.
- Set programmable power supply OFF
- Start data_analysis program and write report file

PSI46 Test file report (1)

2/9/2004 10:34:06 AM

Chip#1

*****Test_1*****

----After reset #1 ---- ----After setup #2 ----

Vdo =1.941V	Vdo =1.873V
Vda =1.903V	Vda =1.859V
Vdg =1.916V	Vdg =1.864V
Vd25=1.949V	Vd25=1.93V
Va16=1.459V	Va16=1.421V
Id25=7.81mA	Id25=25.54mA
Ia16=0.01mA	Ia16=35.55mA

Col=0	Row=0 and 1		
Col=0	Row=0		
UB	1577 1576	1578	2
B	1998 1998	1998	0
LD	2197 2196	2198	2
CO_1	1949 1948	1950	2
C1_1	1909 1908	1910	2
A0_1	2449 2448	2451	3
A1_1	2270 2270	2270	0
A2_1	2496 2494	2497	3
Charge_1	2126 2124	2129	5
Col=0	Row=1		
UB	1577 1576	1578	2
B	1998 1998	1998	0
LD	2197 2196	2198	2
CO_2	1915 1914	1917	3
C1_2	1910 1910	1911	1
A0_2	2449 2448	2450	2
A1_2	2270 2269	2271	2
A2_2	2234 2233	2234	1
Charge_2	2256 2254	2258	4

Report file contains:

- Chip number, date, time.
- Analog and digital supply currents and voltages before and after chip setup.
- Then a statistic on each pixel cell follows. It contains (see left example):
 - Column (0 to 51) and Row (0 to 79) number.
 - Parameter mnemonic (UB = UltraBlack, B = Black, LD = LastDac, CO_1 = Column bit 0 on first pixel, A1_2 = Row bit 1 on second pixel, Charge_1 = Charge on first pixel)
 - Average, Minimum, Maximum and Range (max-min) over all ADC readings (we do 5 readings for each pixel)
- For a valid ADC data see left example. This pixel is considered **PASS** (TestResult(2)=0).

PSI46 Test file report (2)

```
Col=1    Row=14 and 15
1        14        multiple hits response FAIL 832
1        15        multiple hits response FAIL 832
Col=1    Row=16 and 17
1        16        multiple hits response FAIL 820
1        17        multiple hits response FAIL 820
Col=1    Row=18 and 19
1        18        multiple hits response FAIL 1016
1        19        multiple hits response FAIL 1016
Col=1    Row=20 and 21
found fifostat_b=55 FAIL
1        20        not responding FAIL -1
1        21        not responding FAIL -1
Col=1    Row=22 and 23
found fifostat_b=55 FAIL
1        22        not responding FAIL -1
1        23        not responding FAIL -1
```

```
Col=0    Row=0 and 1
0        0        only UB, B, LD response FAIL 40
0        1        only UB, B, LD response FAIL 40
Col=0    Row=2 and 3
0        2        only UB, B, LD response FAIL 40
0        3        only UB, B, LD response FAIL 40
```

```
Col=26   Row=66 and 67
26       66       ambiguous response FAIL 70
26       67       ambiguous response FAIL 70
Col=26   Row=68 and 69
26       68       ambiguous response FAIL 72
26       69       ambiguous response FAIL 72
```

- If the ADC data is not valid, one of the following failures occurs:
 - If there is no token out, that pixel pair is qualified as **'not responding FAIL'** (TestResult(2)=1)
 - If there is token out but no pixel response, that pixel pair is qualified as **'only UB, B, LD response FAIL'** (TestResult(2)=2)
 - If only one cell out of two is responding, that pixel pair is qualified as **'only one row response FAIL'** (TestResult(2)=3)
 - If more than two hits are received, that pixel pair is qualified as **'multiple hits response FAIL'** (TestResult(2)=4)
 - All other cases are qualified as **'ambiguous response FAIL'** (TestResult(2)=5)
- NOTE: The number after FAIL is related to the ADC/FIFO word count received.

```
Col=13   Row=42 and 43
found fifostat_b=55 FAIL
13       42       not responding FAIL -1
13       43       not responding FAIL -1
Col=13   Row=44 and 45
found fifostat_b=55 FAIL
13       44       not responding FAIL -1
13       45       not responding FAIL -1
```

PSI46 Test file report (3)

column and row repeatability is <7

Column Levels

CO_L0	1954	1918	1988	70
CO_L1	2080	2044	2108	64
CO_L2	2214	2178	2251	73
CO_L3	2338	2305	2371	66
CO_L4	2444	2407	2464	57
C1_L0	1973	1943	2003	60
C1_L1	2091	2050	2131	81
C1_L2	2215	2184	2247	63
C1_L3	2337	2305	2370	65
C1_L4	2446	2414	2478	64
C1_L5	2535	2501	2568	67

Row Levels

A0_L0	1971	1924	2017	93
A0_L1	2099	2051	2146	95
A0_L2	2232	2184	2279	95
A0_L3	2354	2305	2400	95
A0_L4	2463	2414	2511	97
A1_L0	1967	1923	2005	82
A1_L1	2093	2051	2134	83
A1_L2	2226	2183	2266	83
A1_L3	2338	2304	2373	69
A1_L4	2447	2413	2480	67
A1_L5	2536	2500	2570	70
A2_L0	1971	1924	2017	93
A2_L1	2099	2052	2145	93
A2_L2	2230	2183	2277	94
A2_L3	2352	2304	2400	96
A2_L4	2461	2412	2510	98
A2_L5	2549	2499	2596	97

Universal Levels

L0	1918	2017	99	
L1	2044	2146	102	27
L2	2178	2279	101	32
L3	2304	2400	96	25
L4	2407	2511	104	7
L5	2499	2596	97	-12

- After all pixels were reported as described, a kind of summary follows.
- The **ADC measurement repeatability** is reported. It is defined as the maximum range value, over all 4160 pixels, for all Column and Row address readings, for all 5 readings. The UB, B, LD and Charge ranges are not considered.
- Starting from Column and Row average ADC data for each pixel (see previous slide description), the **five/six analog levels** (L0, L1, L2, L3, L4, L5) are extracted: average, min, max and range over all pixels that provided good ADC data (PASS). This is done for each 'bit' at a time, i.e. C0, C1, A0, A1 and A2.
- Then a kind of '**Six Universal Levels**' are inferred, regardless of column or row address provenience (see left example). The first value is the minimum over all associated columns and row level, the second column is the maximum, then the range, and the last column is the 'gap' between two consecutive levels. We can see from the (typical) left example that the analog level range is about 100 counts wide, with a separation of >25 counts between L0, L1, L2 and L3. This is decreased to 7 counts between L3 and L4 and finally L5 overlaps L4 with 12 counts.
- The last part of the report is just a listing of all pixels (if any) that failed (see previous slide categories) : pixel column, row, type of failure

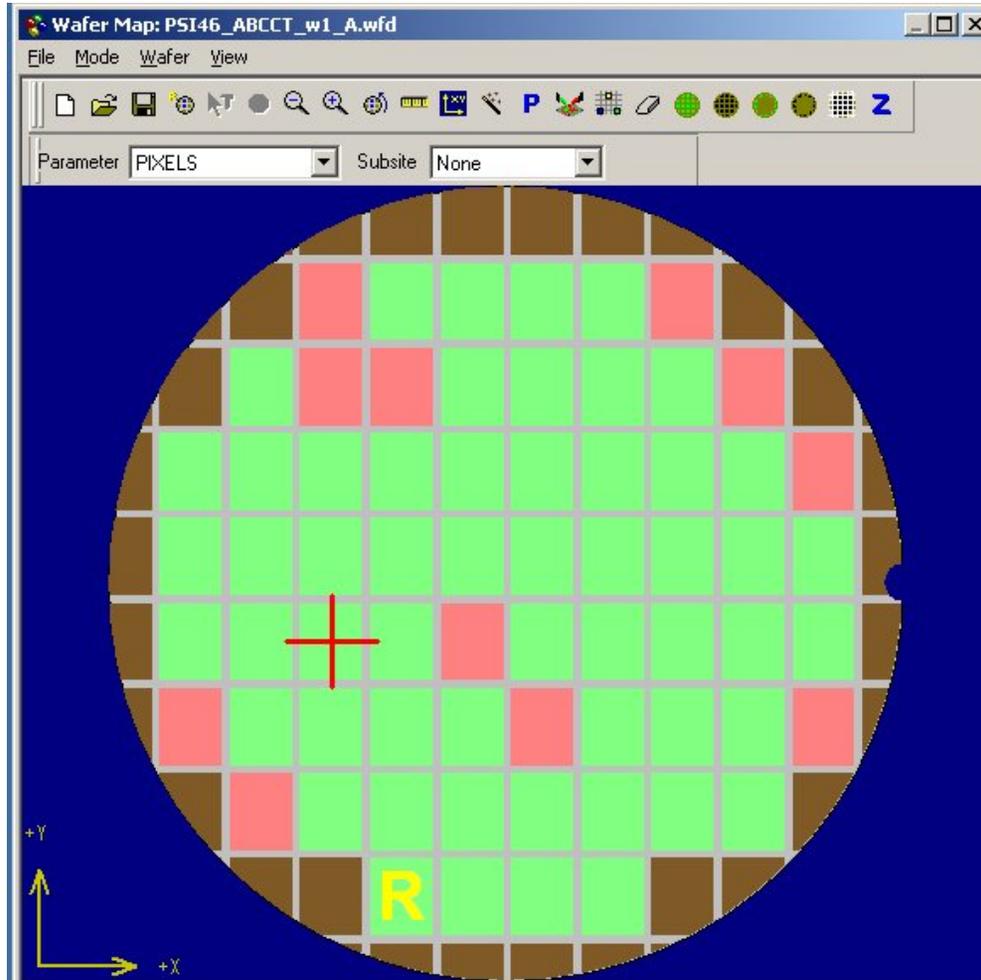
```

1      76      only UB, B, LD response 40
1      77      only UB, B, LD response 40
1      78      only UB, B, LD response 40
1      79      only UB, B, LD response 40
160 pixels FAIL
L4_max >= L5_min overlap FAIL
**** END OF TEST ****
    
```

```

REPORTING FAILED PIXELS
all pixels PASS
L4_max >= L5_min overlap FAIL
**** END OF TEST ****
    
```

Wafer testing results (1)



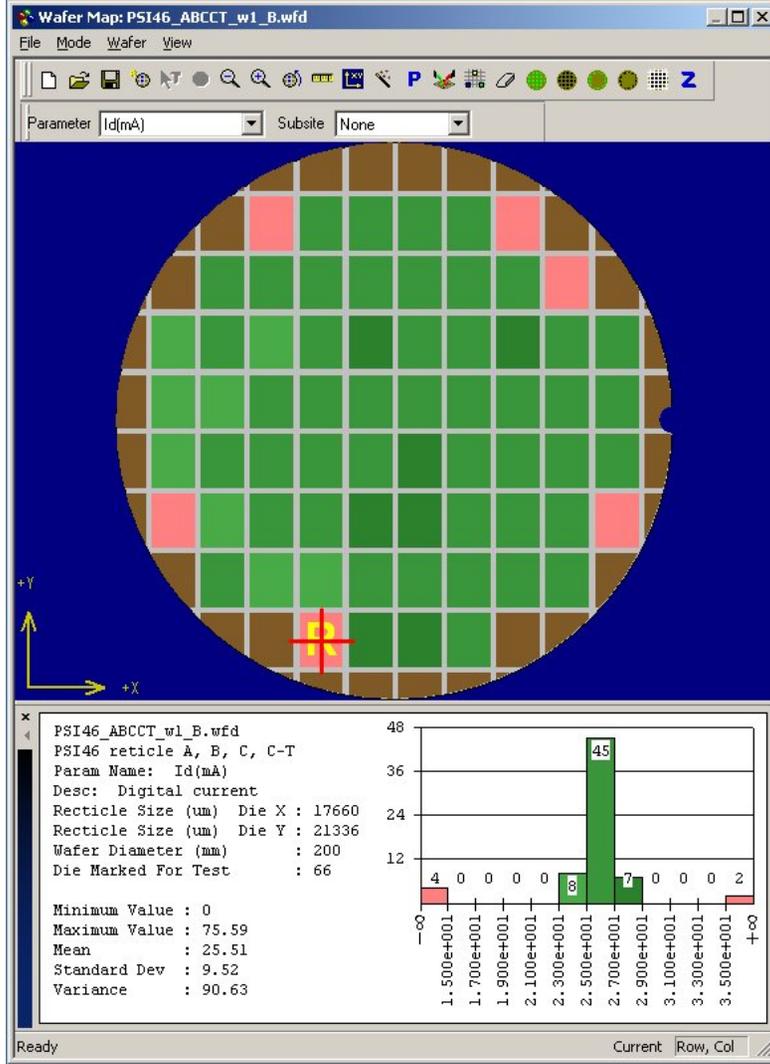
- During testing, NUCLEUS Wafer Map is updated with testing results. This is convenient for 'in time' visual check of test status.
- There are six TestResult(1 to 6) numbers that can be monitored during wafer testing:
 - **TestResult(1) = ADC/FIFO status** -> 0 if no errors, +1 if fifostat_b error, +2 if fifostat_e error
 - **TestResult(2) = ADC word count** -> 0 = no errors, 1 = pixel not responding, 2 = only UB, B, LD response, 3 = only one pixel response, 4 = multiple hits, 5 = ambiguous response
 - **TestResult(3) = Analog Levels Overlap** -> 0 if no errors, +1 if L0_max > L1_min, +2 if L1_max > L2_min, +4 if L2_max > L3_min, +8 if L3_max > L4_min, +16 if L4_max > L5_min
 - **TestResult(4) = Pixels** -> 0 = all pixels PASS, n = 1 to 4160 if n pixels FAIL
 - **TestResult(5) = Id(mA)** -> digital current supply in mA
 - **TestResult(6) = Ia(mA)** -> analog current supply in mA
- **Convention used for chip number:** Chip ID number = 1 in position (R), then increase by one as going from left to right in one row. Rows are measured from bottom to top. There are 66 recticles per wafer.

Wafer testing results (2)

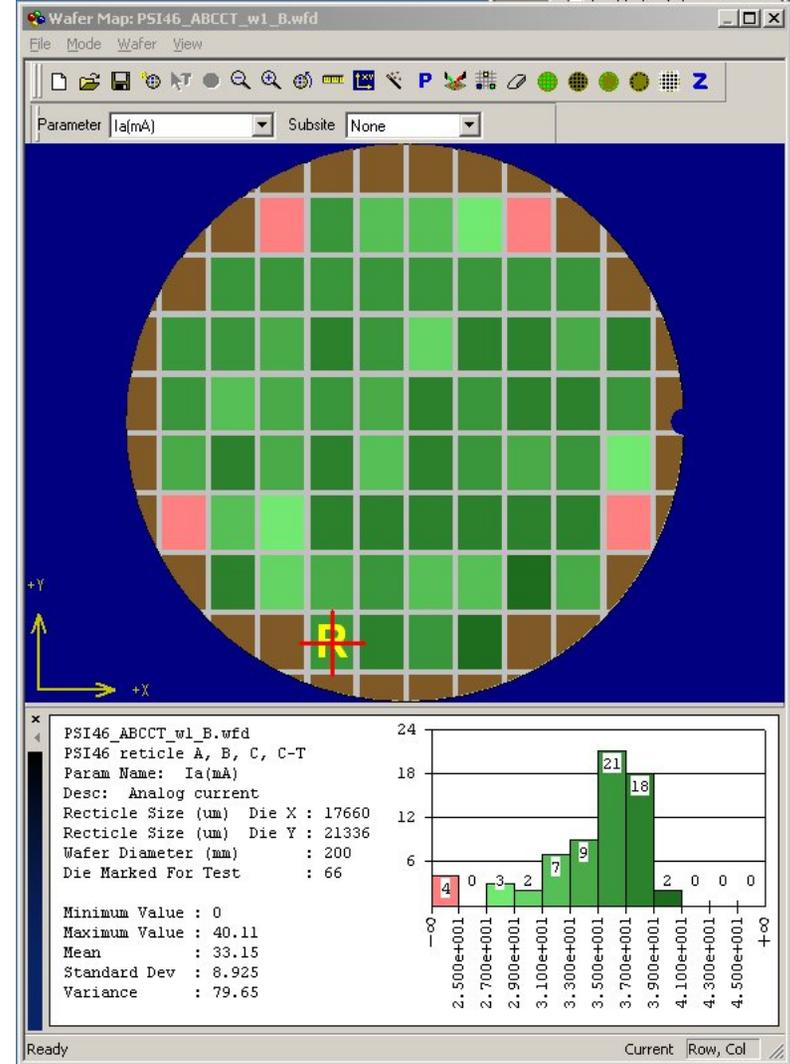
PSI46 - wafer 1 - version A - Failure summary

- All chips had **L4_max >= L5_min overlap FAIL**
- **Chip#5** 160 pixels failed (col1 and col2, all with failure type 'only UB, B, LD response'
RETESTED => identical result, same 162 pixels failed same way **MARGINAL**
- **Chip#13** **not responding** =>all 4160 pixels failed and **Ia=Id=0mA** **DEAD**
- **Chip#18** 4160 pixels failed in different ways,
RETESTED=>276 pixels failed in different ways
This chip might need special DAC settings (?) **MARGINAL**
- **Chip#22** **not responding** =>all 4160 pixels failed and **Ia=Id=0mA** **DEAD**
- **Chip#27** **only UB, B, LD response** =>all 4160 pixels failed
RETESTED => identical result Id=36mA, Ia=35mA **DEAD**
- **Chip#52** 4160 pixels failed in different ways, **Ia=0mA, Id=9mA**
RETESTED => all pixels **PASS** **PASS!!!**
RETESTED again => all pixels **PASS** **PASS!!!**
- **Chip#54** 480 pixels failed with **only UB, B, LD response**
RETESTED => identical results (col22,23,26,27,28 and 29)
This chip might need special DAC settings (?) **MARGINAL**
- **Chip#55** 990 pixels failed with **only UB, B, LD response**, (col39, row51 to end)
RETESTED => 960 pixels failed with **only UB, B, LD response** (col40 to 51)
This chip might need special DAC settings (?) **MARGINAL**
- **Chip#60** **not responding** =>all 4160 pixels failed and **Ia=0mA** **DEAD**
- **Chip#61** **not responding** =>all 4160 pixels failed and **Ia=Id=0mA** **DEAD**
- **Chip#66** **not responding** =>all 4160 pixels failed and **Ia=Id=0mA** **DEAD**

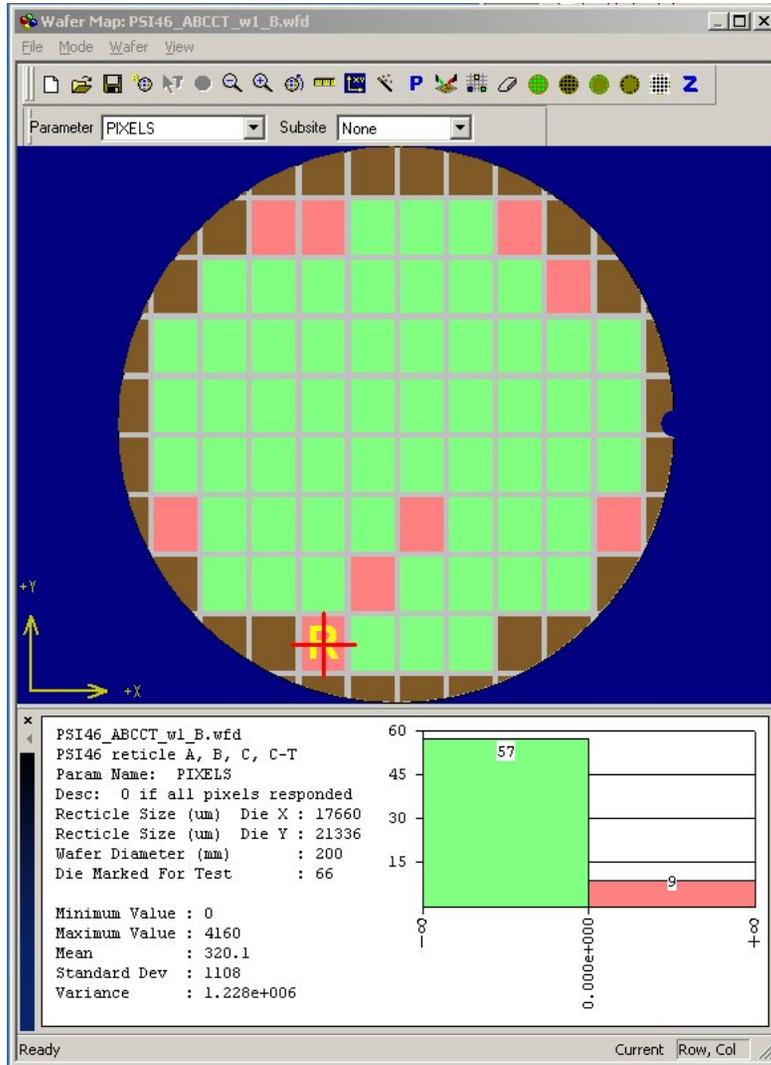
Wafer testing results (3)



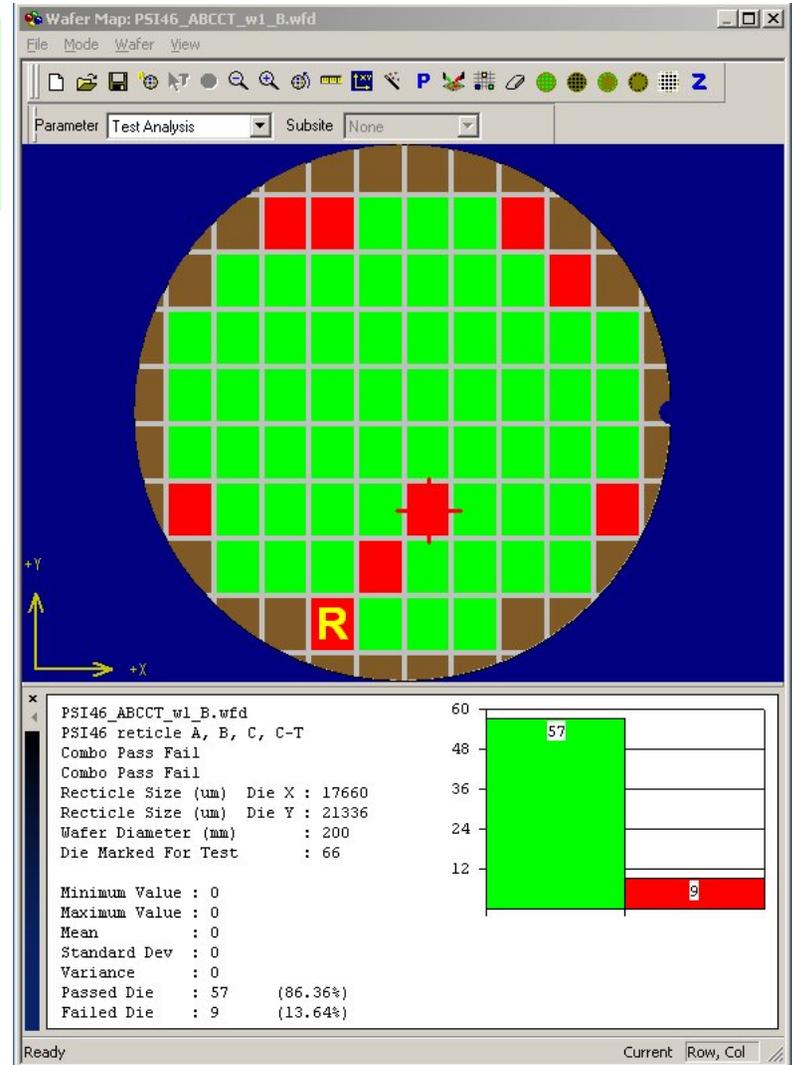
PSI46
waf.1
ver.B



Wafer testing results (4)



PSI46
waf.1
ver.B

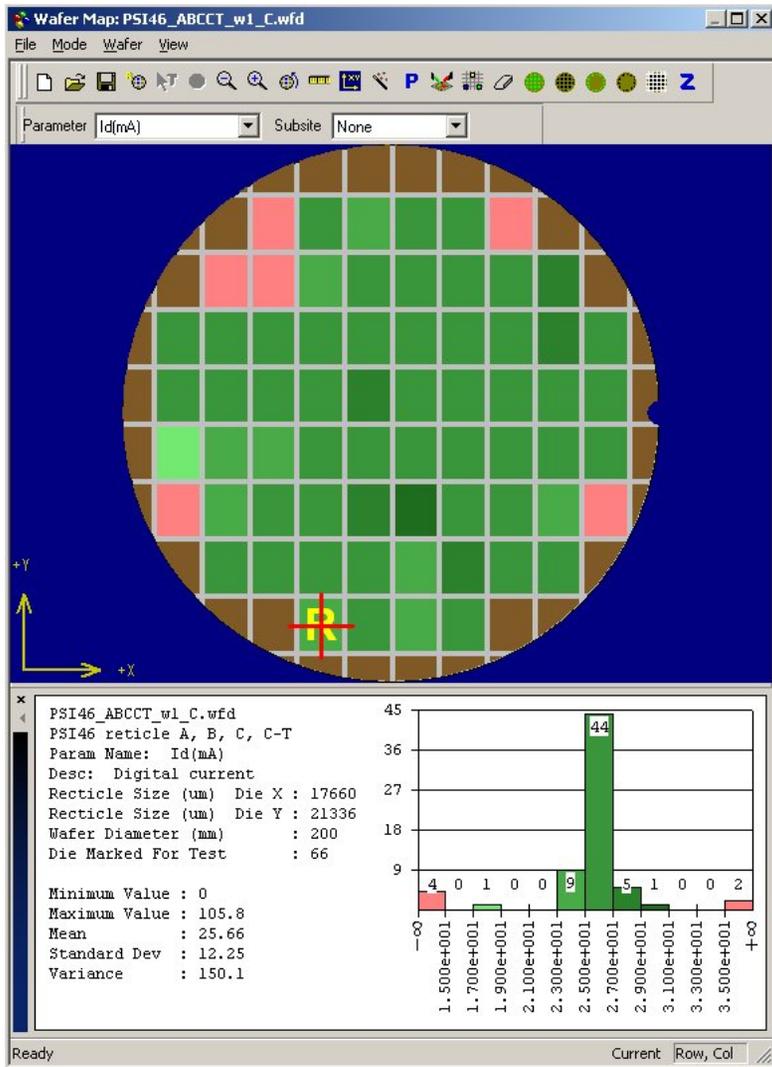


Wafer testing results (5)

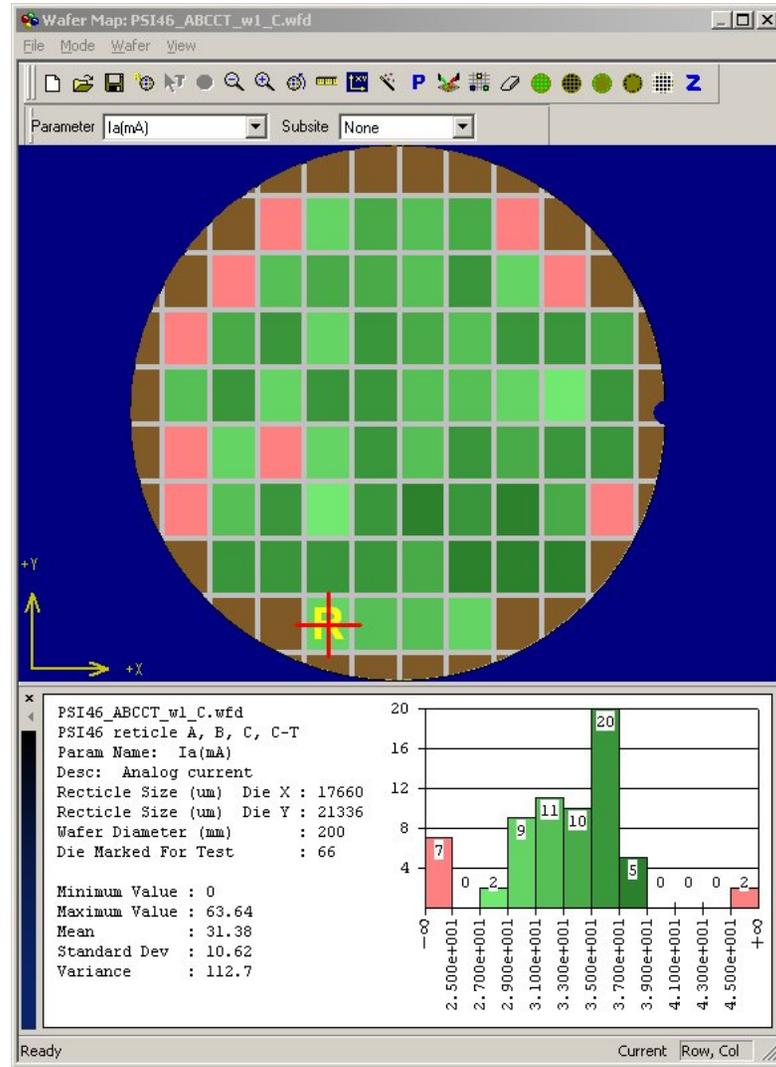
PSI46 - wafer 1 - version B - Failure summary

- All chips had **L4_max >= L5_min overlap FAIL**
- **Chip#1** **not responding** =>all 4160 pixels failed **BUT Ia=35mA, Id=76mA**
RETESTED => identical result, **BUT** on the scope you can see pixels' analog response WITOUT token-out signal present (because of high value of Id?) **MARGINAL**
- **Chip#8** 2 pixels failed (col32, row60,61, failure type is 'ambiguous response FAIL 148')
RETESTED => all pixels **PASS** **PASS**
- **Chip#13** **not responding** =>all 4160 pixels failed and **Ia=Id=0mA** **DEAD**
- **Chip#18** 2 pixels failed (col11, row20,21, failure type 'only one row response')
RETESTED => identical result, same 2 pixels failed same way. **MARGINAL**
- **Chip#22** **not responding** =>all 4160 pixels failed and **Ia=Id=0mA** **DEAD**
- **Chip#60** 162 pixels failed (in col46,47,51 with different failure types: 'only UB, B, LD' or 'ambiguous response' or 'only one row response') and Ia=35mA, Id=52mA
RETESTED => now 250 pixels failed (this includes previous 162 but now with slightly different failure types each) and Ia=33mA, Id=50mA **MARGINAL**
- **Chip#61** **not responding** =>all 4160 pixels failed and **Ia=Id=0mA** **DEAD**
- **Chip#62** 162 pixels failed (col41, row20,21 and col42 and 43 all rows, all with 'only UB, B, LD')
RETESTED => identical result, same 162 pixels failed same way **MARGINAL**
- **Chip#66** **not responding** =>all 4160 pixels failed and **Ia=Id=0mA** **DEAD**

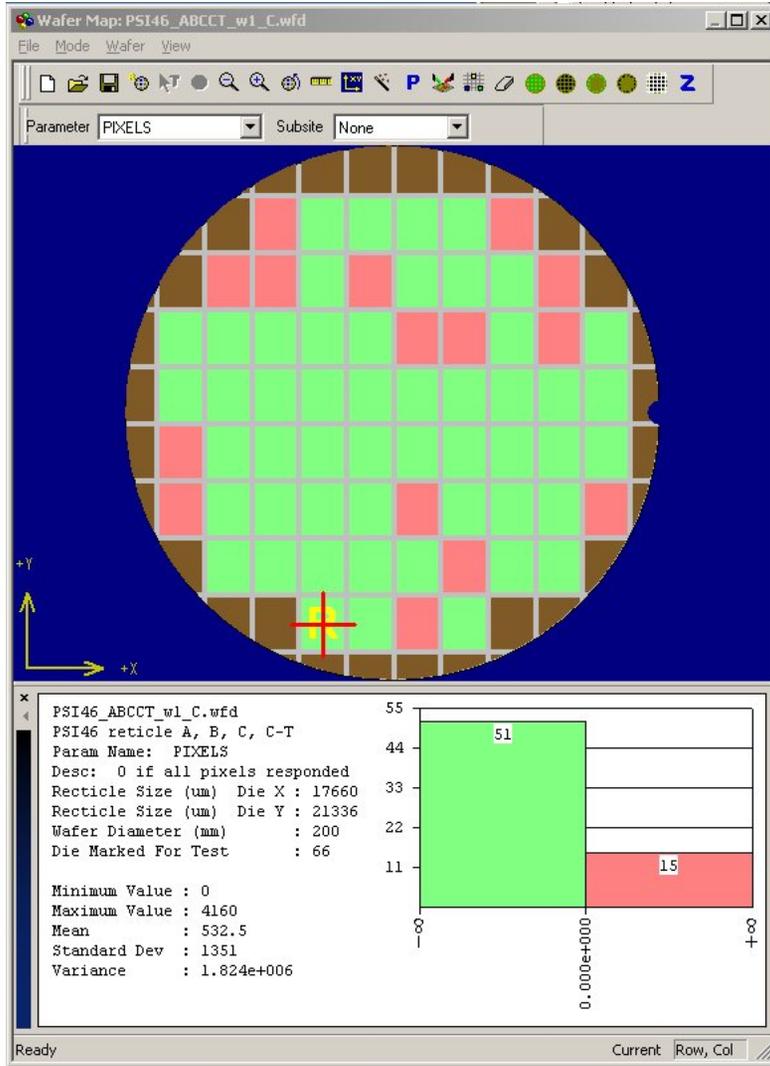
Wafer testing results (6)



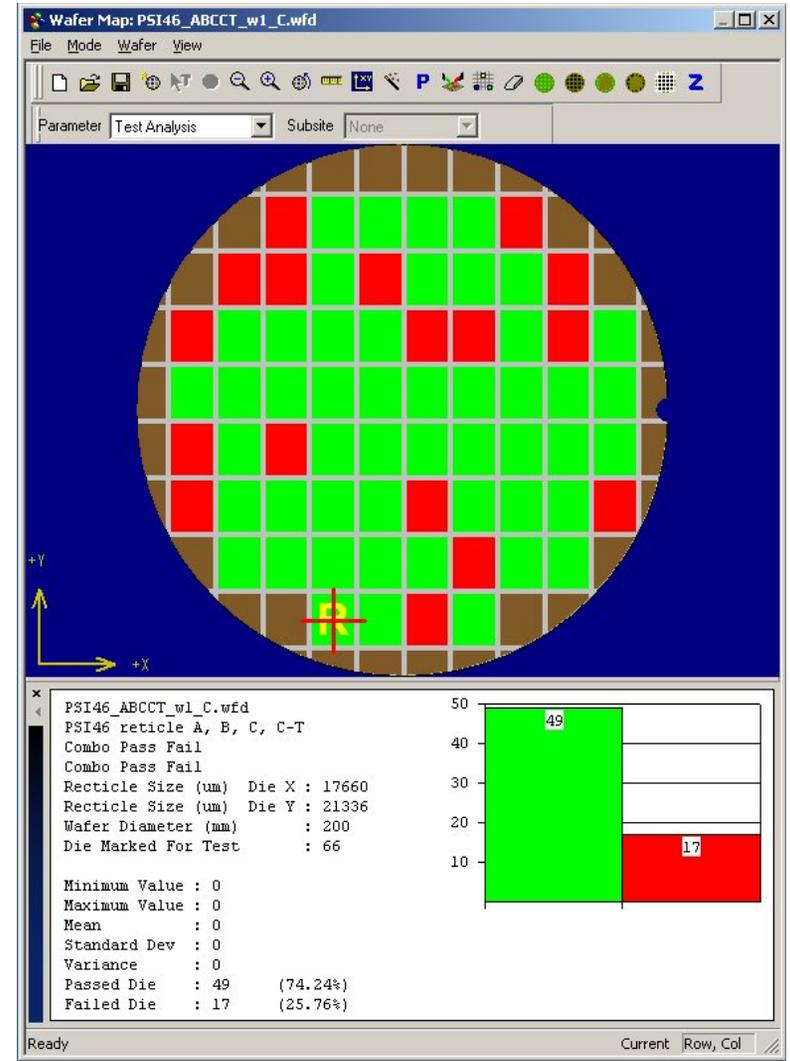
PSI46
waf.1
ver.C



Wafer testing results (7)



PSI46
waf.1
ver.C



Wafer testing results (8)

PSI46 - wafer 1 - version C - Failure summary

- All chips had **L4_max >= L5_min overlap FAIL**
- Chip#3 2 pixels failed (col27, row6,7, only one row responding)
RETESTED => identical result, same pixels failed same way **MARGINAL**
- Chip#10 160 pixels failed (col0 and col1, only UB, B, LD)
RETESTED => all 4160 pixels failed 'not responding' **MARGINAL**
- Chip#13 **not responding =>all 4160 pixels failed and Ia=Id=0mA**
RETESTED => identical result, same pixels failed same way **DEAD**
- Chip#18 3840 pixels failed (col4,5 'only UB, B, LD', col6 to 51 'not responding')
RETESTED => identical result, same pixels failed same way **DEAD**
- Chip#22 **not responding =>all 4160 pixels failed and Ia=Id=0mA**
RETESTED => identical result, same pixels failed same way **DEAD**
- Chip#23 **not responding =>all 4160 pixels failed and Ia=0mA, Id=17mA**
RETESTED => identical result, same pixels failed same way **DEAD**
- Chip#48 152 pixels failed (from col48, row8 to col49, row79, 'only UB, B, LD')
RETESTED => identical result, same pixels failed same way **MARGINAL**
- Chip#49 160 pixels failed (col12,13, 'only UB, B, LD')
RETESTED => identical result, same pixels failed same way **MARGINAL**
- Chip#51 114 pixels failed (col20 and 21, rows 24 to 79, 'only UB, B, LD')
RETESTED => identical result, same pixels failed same way **MARGINAL**
- Chip#53 **not responding =>all 4160 pixels failed and Ia=63mA, Id=106mA**
RETESTED => identical result, same pixels failed same way **DEAD**
- Chip#54 640 pixels failed (col10 to 17, row0 to 79, 'only UB, B, LD')
RETESTED => identical result, same pixels failed same way **DEAD**
- Chip#56 960 pixels failed (col40 to 51, 'only UB, B, LD')
RETESTED => identical result, same pixels failed same way **DEAD**
- Chip#60 4160 pixels failed in mixed ways and **Ia=28mA, Id=53mA**
RETESTED => similar mixed failures result **DEAD**
- Chip#61 **not responding =>all 4160 pixels failed and Ia=Id=0mA**
RETESTED => identical result, same pixels failed same way **DEAD**
- Chip#66 **not responding =>all 4160 pixels failed and Ia=Id=0mA**
RETESTED => identical result, same pixels failed same way **DEAD**

Wafer testing results (9)

PSI46 - wafer 1 - version CT - Failure summary

- All chips had 328 pixels failed this way: no response from col48 to 51 (320 pixels) and col6 and 7 row0 and 1 (4 pixels) with only UB, B, LD; for col6 and 7 row2 and 3 only one row response (4 pixels)
- Because of previous failure type, apart from the usual L4_max >= L5_min overlap we have also a report of L3_max >= L4_min
- The following summary reports all pixels failed (including the above 328) but the failure type is reported only for the extra pixels failed

- Chip#10 2410 pixels failed (col22 to 51 with no response and col15 row4,5 only one row responding)
RETESTED => identical result, same pixels failed same way **DEAD**
- **Chip#13 not responding =>all 4160 pixels failed and Ia=Id=0mA** **DEAD**
- Chip#14 330 pixels failed (col17, row52, 53, only one row responding)
RETESTED => identical result, same pixels failed same way **MARGINAL**
- Chip#17 1814 pixels failed (misc. pixels and failures) Ia=31mA, Id=48mA
RETESTED => 1816 pixels failed **DEAD**
- Chip#18 330 pixels failed (col9, row46,47, only one row responding)
RETESTED => identical result, same pixels failed same way **MARGINAL**
- **Chip#22 not responding =>all 4160 pixels failed and Ia=Id=0mA** **DEAD**
- Chip#26 330 pixels failed (col14, row72,73, only one row responding)
RETESTED => identical result, same pixels failed same way **MARGINAL**
- Chip#60 488 pixels failed (col22,23, only UB, B, LD)
RETESTED => identical result, same pixels failed same way **MARGINAL**
- **Chip#61 not responding =>all 4160 pixels failed and Ia=Id=0mA** **DEAD**
- **Chip#66 not responding =>all 4160 pixels failed and Ia=Id=0mA** **DEAD**

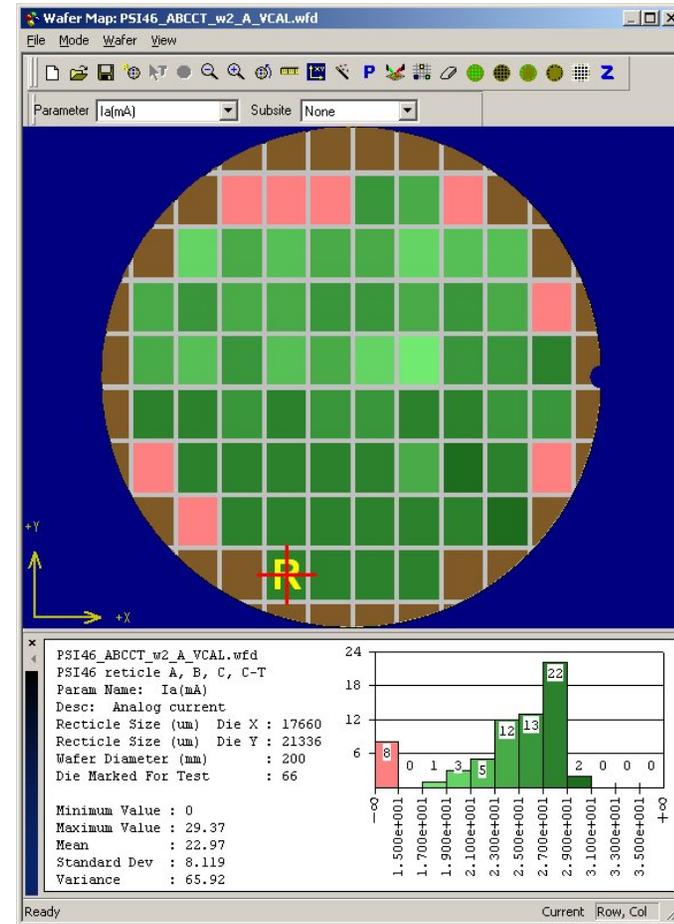
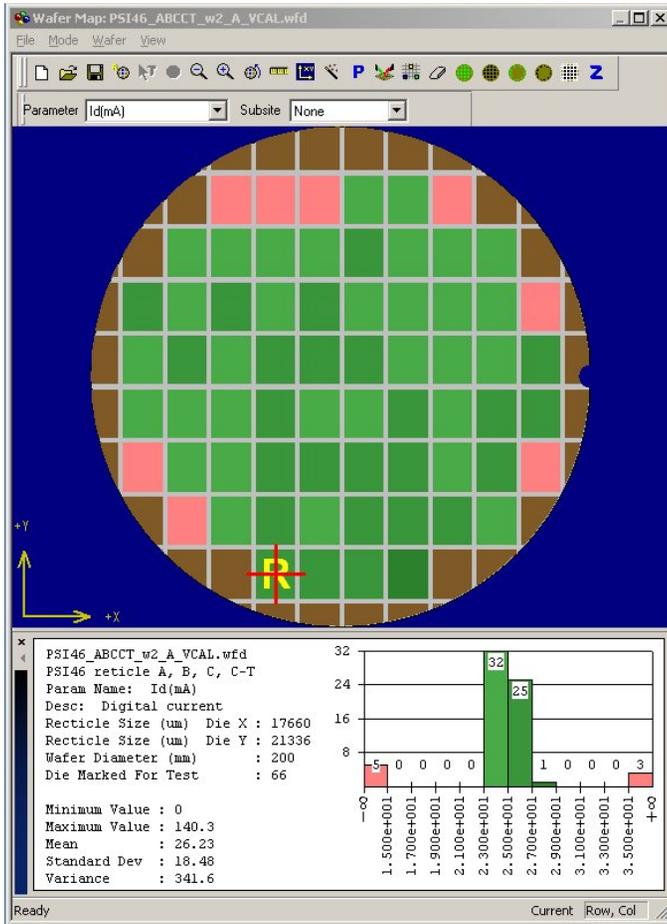
PSI46 - wafer 1 - all versions Yield summary

- Considering as FAIL all previous chips categorized as DEAD or MARGINAL, the yield on wafer 1 is:
- **Version A** (66-10)/66 = **84.84%**
- **Version B** (66-8)/66 = **87.87%**
- **Version C** (66-15)/66 = **77.27%**
- **Version CT** (66-10)/66 = **84.84%**

Wafer testing results (14)

PSI46 - wafer 2 - version A - Ia

Note that comparing with wafer 1, digital supply current has a similar distribution (15 to 35mA centered around 25mA) but the analog supply current distribution is shifted about 10mA down, between 15 to 35mA centered around 25mA instead of 25 to 45mA centered around 35mA.



Wafer testing results (15)

PSI46 - wafer 2 - version A - Failure summary

- Chip#24,50 with 2 respectively 160 pixels failed (only one row responding)
RETESTED => identical result, same pixels failed same way for all VCAL MARGINAL
- Chip#51 4160 pixels failed with ambiguous response, Id=9mA, Ia=0mA
RETESTED => PASS when VCAL=64 and 96, 2pixels failed (multiple hits) when VCAL=128,
38pixels failed (multiple hits) when VCAL=160 MARGINAL
- Chip#60 76,72,70,77 pixels failed in col35 when VCAL=64,96,128 respectively 160 (only UB,B,LD)
RETESTED => 76,74,72,72 pixels failed in col35 when VCAL=64,96,128,160 MARGINAL
- Chips#5,13,22,43,52,61,62,63,66 not responding =>all 4160 pixels failed DEAD

PSI46 - wafer 2 - version B - Failure summary

- Chip#1 422 pixels failed
RETESTED => 118,38,PASS,PASS pixels failed when VCAL=64,96,128 respectively 160 MARGINAL
- Chip#18,20 with 2 respectively 160 pixels failed (only one row responding) on all VCAL values
RETESTED => identical result, same pixels failed same way for all VCAL MARGINAL
- Chips#12,13,22,52,61,62,63,66 not responding =>all 4160 pixels failed DEAD

PSI46 - wafer 2 - version C - Failure summary

- Chip#1 PASS,PASS,152,820 pixels failed when VCAL=64,96,128 respectively 160
RETESTED => PASS for all VCAL MARGINAL
- Chip#8 with 118,160,160,160 pixels failed when VCAL=64,96,128 respectively 160
RETESTED => identical result, same pixels failed same way MARGINAL
- Chip#12 with 2,2,2,2 pixels failed when VCAL=64,96,128 respectively 160 (col10 row24,25 only one row response)
RETESTED => identical result, same pixels failed same way MARGINAL
- Chip#27 with 2 pixels failed when VCAL=64 (col14 row54,55 ambiguous response)
RETESTED => identical result, same pixels failed same way MARGINAL
- Chip#52 with 2,2,2,2 pixels failed when VCAL=64,96,128 respectively 160 (col35 row78,79 only one row response)
RETESTED => identical result, same pixels failed same way MARGINAL
- Chips#13,22,42,43,54,55,61,62,63,66 not responding =>all 4160 pixels failed DEAD

Wafer testing results (16)

PSI46 - wafer 2 - version CT - Failure summary

- All chips had 328 pixels failed this way: only UB,B,LD from col48 to 51 (320 pixels) and col6 and 7 row0 and 1 (4 pixels) with only UB, B, LD; for col6 and 7 row2 and 3 only one row response (4 pixels)
- The following summary reports the extra pixels failed with their failure type
- Chip#39 +160 pixels failed on all VCAL values (col30 and 31, only UB,B,LD)
RETESTED => identical result, same pixels failed same way for all VCAL MARGINAL
- Chip#50 +160 pixels failed on all VCAL values (col4 and 5, mixed failures)
RETESTED => identical result MARGINAL
- Chips#13,22,32,54,55,61,62,63,66 not responding =>all 4160 pixels failed DEAD

PSI46 - wafer 2 - all versions Yield summary

- Considering as FAIL all previous chips categorized as DEAD or MARGINAL, the yield on wafer 1 is:
- Version A $(66-13)/66 = 80.30\%$
- Version B $(66-11)/66 = 83.33\%$
- Version C $(66-15)/66 = 77.27\%$
- Version CT $(66-11)/66 = 83.33\%$

PSI46 - wafer 1 and 2 general comments

- Wafer 1 ID is ARCN8QX
- Wafer 2 ID is A3CN6EX
- Some chip (rectangle) numbers fail almost on all versions, like for example #13 or #61, 62, 63 and 66. While it can be verified that, say, #13 version A is located on the edge of the wafer and it has indeed some pads missing and thus will always fail, this is not a common explanation.