

# PSI43 Test Setups at FNAL

## Two types of setups

- **Wafer test stand (Boris & ASIC group)**
- **FPGA TBM based test stand (Rutgers) to test VHDI mounted ROCs**



# PSI43 Test Setups at FNAL

- **ROC wafer test stand at WH14E**
  - Based on EED ASIC Test System and Cascade/Alessi 6171 semi-automatic 8 inch chuck probe station
  - Two additional boards designed to interface to the ROC:
    - **ASIC Interface Board features interface to the ASIC Test System, two timing sequencers to generate calibrate/trigger/reset signal and pseudo I2C commands, programmable power supplies and fast ADC to digitize analog data output**



ASIC Interface Board



# PSI43 Test Setups at FNAL

- **PSI43 Buffer Board (not to scale) mounted on Rucker & Kolls probe card features level converters from standard CMOS and LVDS to negative CMOS and negative LVDS levels**

PSI43 Buffer Board



- **Allows manual and semi-automated wafer and single chip testing**



ASIC Test System with PSI43 boards attached



ROC Wafer Test Stand at WH14E

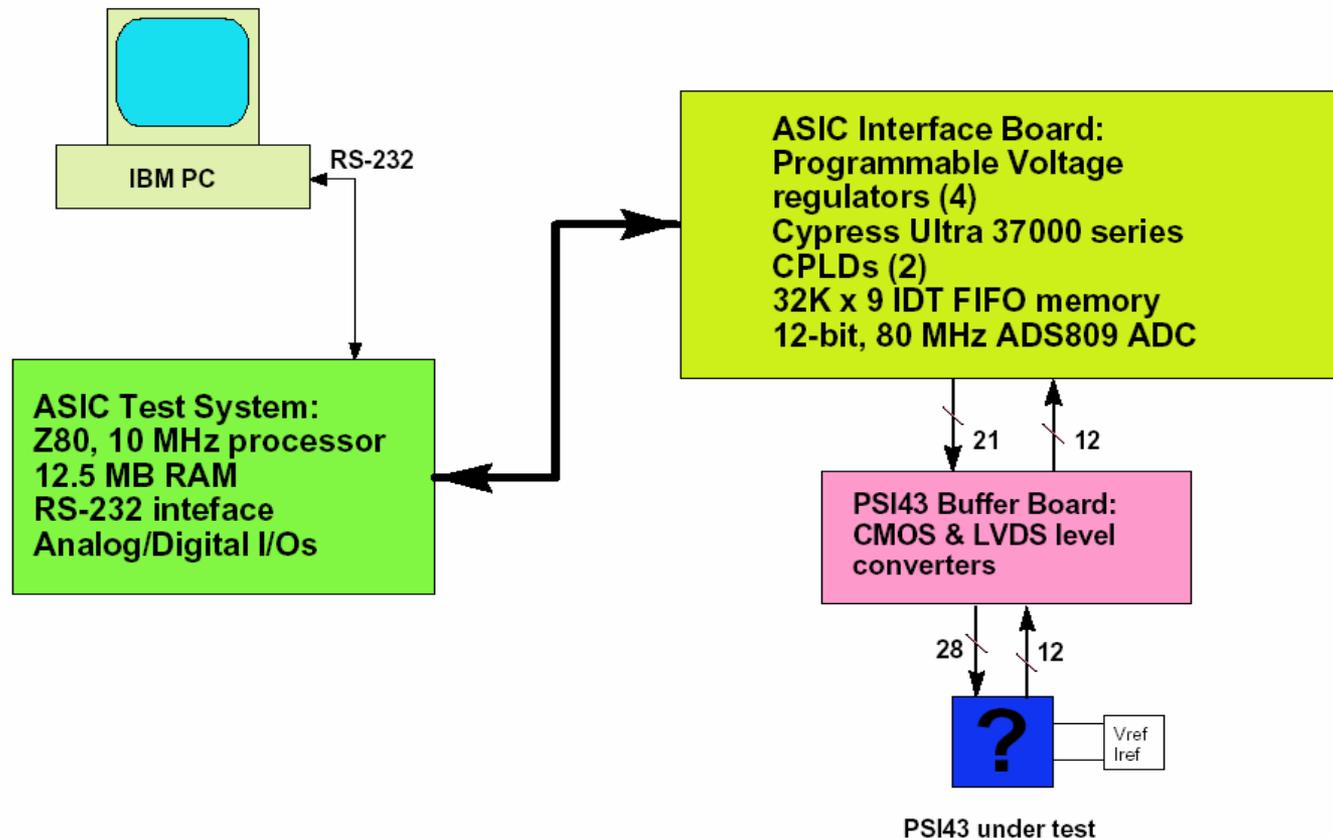


# PSI43 Test Setups at FNAL

- Block-diagram of the ROC wafer test stand

PSI43 Wafer Test Stand

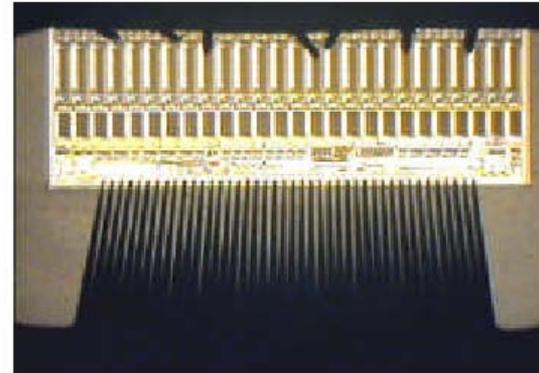
B.Baldin  
03/04/03



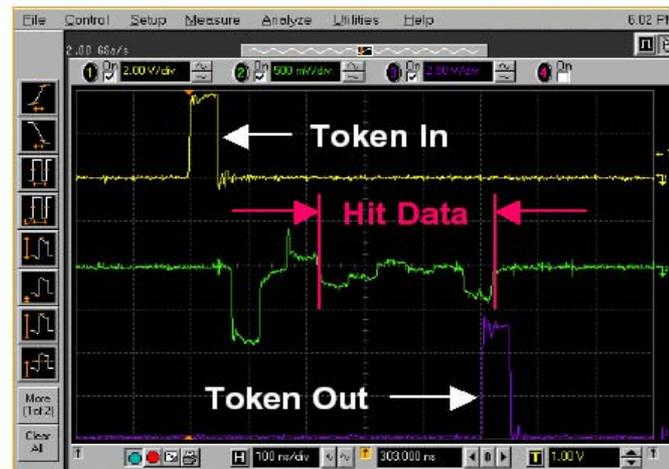


# PSI43 Test Setups at FNAL

- Photograph of the wire probes on PSI43 pads (42 probes @ 150  $\mu$  pitch)



- PSI43 #9 response to a single cell calibration trigger sequence





# PSI43 Test Setups at FNAL

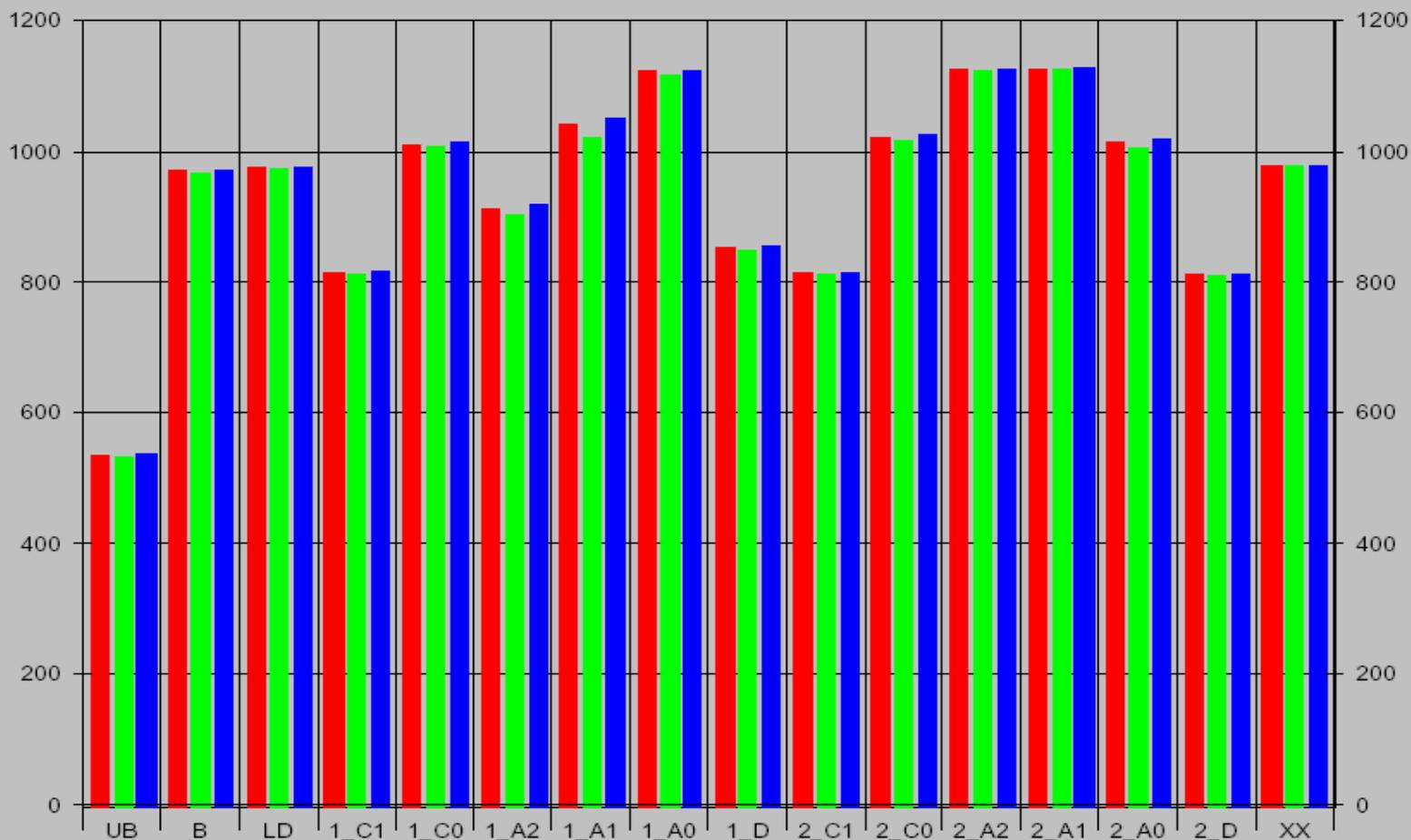
## Preliminary ROC chip test results

- Tested 48 single diced chips and 31 chips on wafer
  - Used loose test procedure to select “working” chips as following:
    - Currents and voltages are within expected range
    - Responded to the serial control interface commands (Last programmed DAC value changing)
    - Two or more (out of 26) double columns responded to the calibration trigger sequence
  - Tested several varieties of the chip:
    - 31 chips on wafer, yield ~ 42%
    - 31 diced chips, yield ~ 45%
    - 17 diced and bump bonded chips, yield ~ 59%



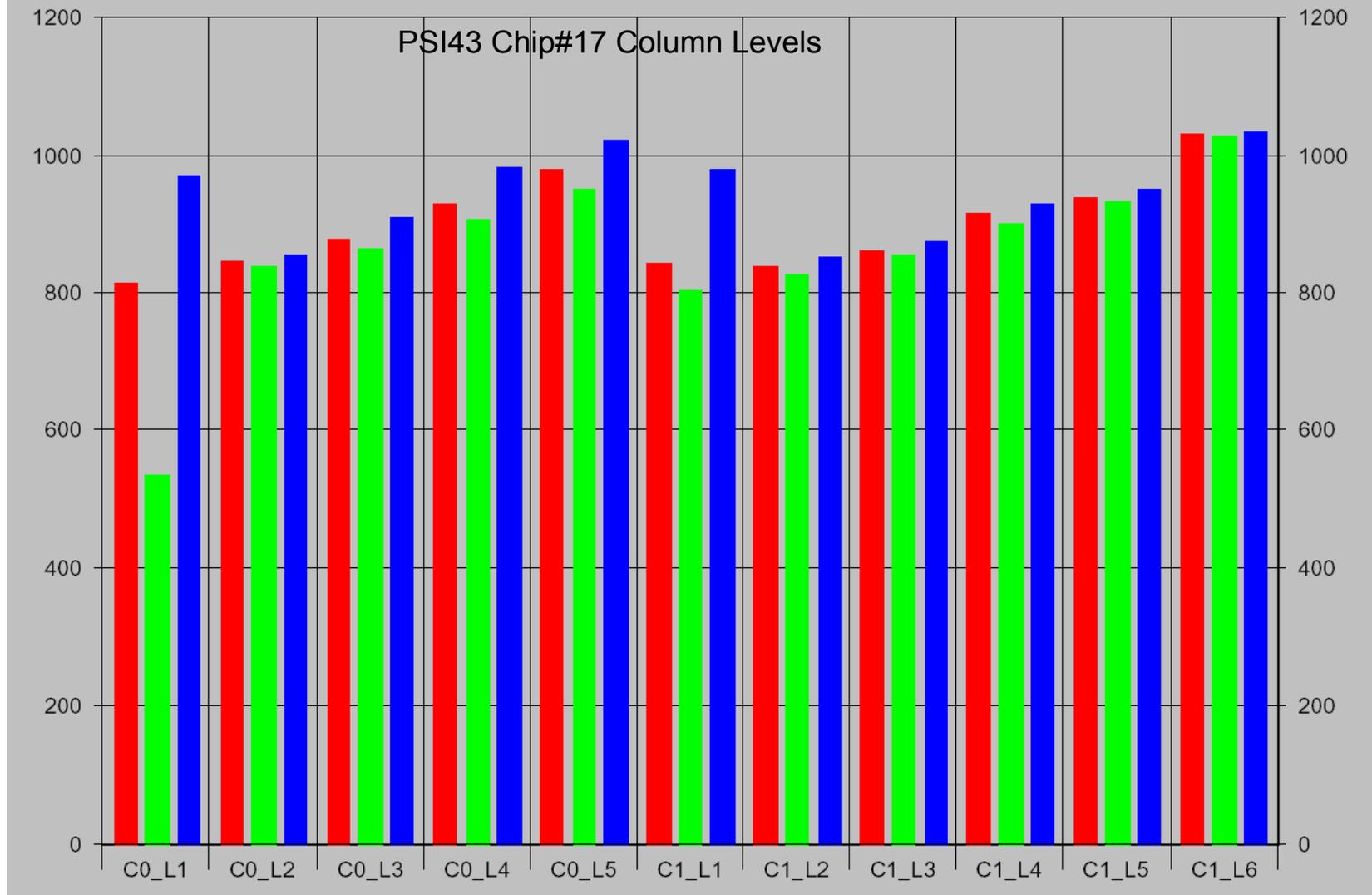
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PSI43 Chip#17 Double Column #5



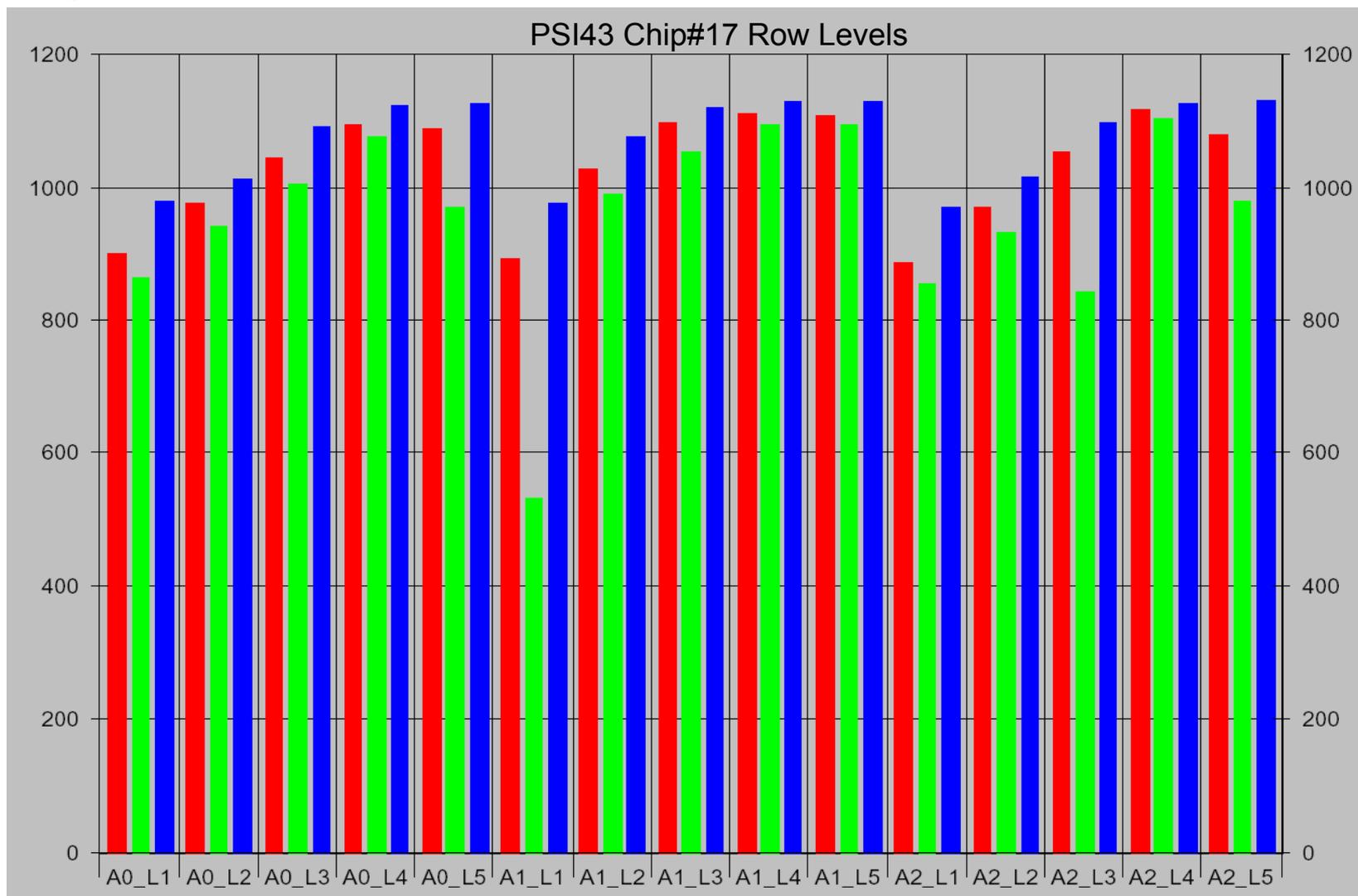


# PSI43 Test Setups at FNAL



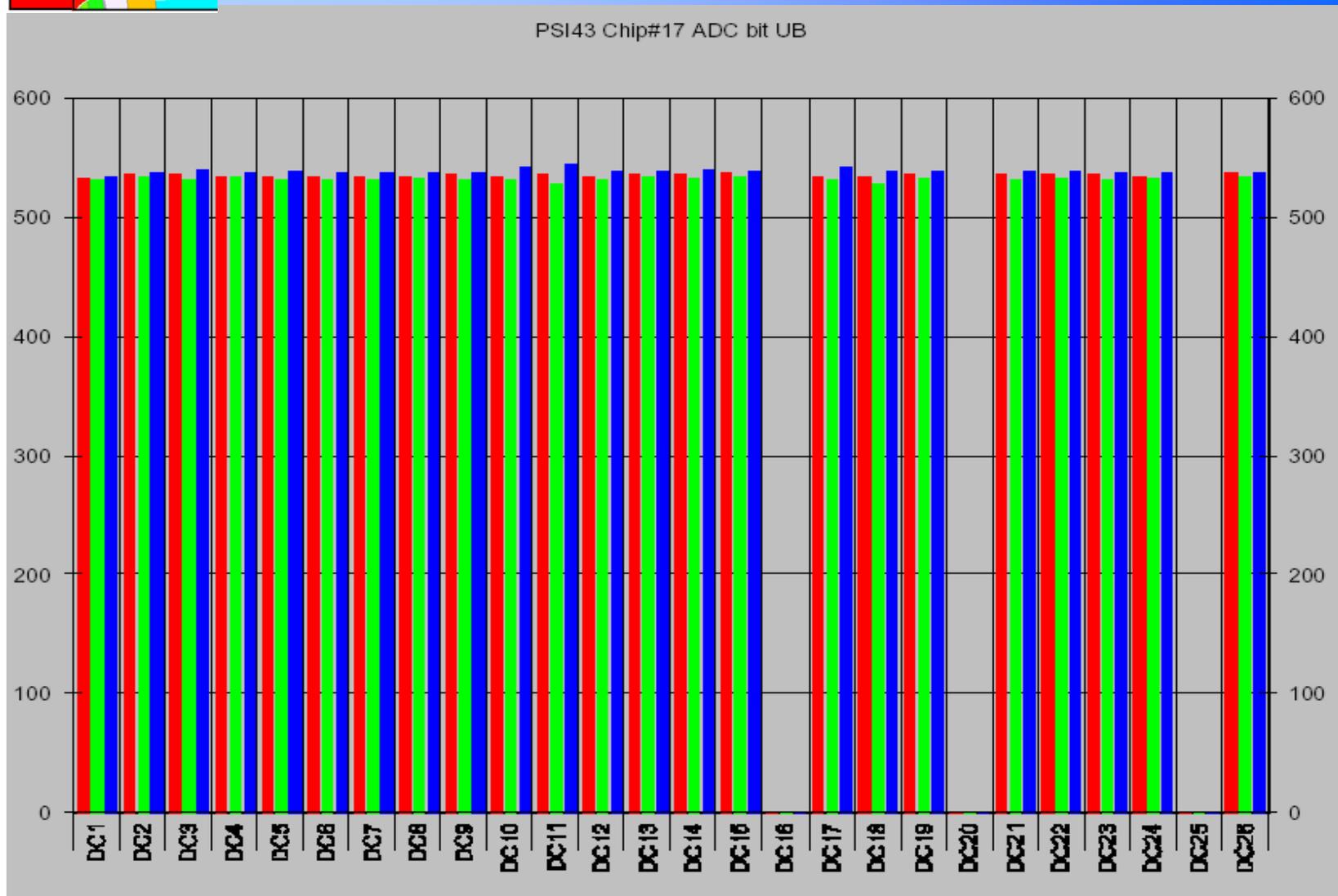


# PSI43 Test Setups at FNAL





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# PSI43 Test Setups at FNAL

## Infrastructure for ROC testing at FNAL

- Rutgers University test fixture (FPGA TBM) for VHDI tests (two available at SiDet, FNAL)
  - Requires HDI adapter board to connect the VHDI
  - Allows various tests on ROC chips mounted on VHDI



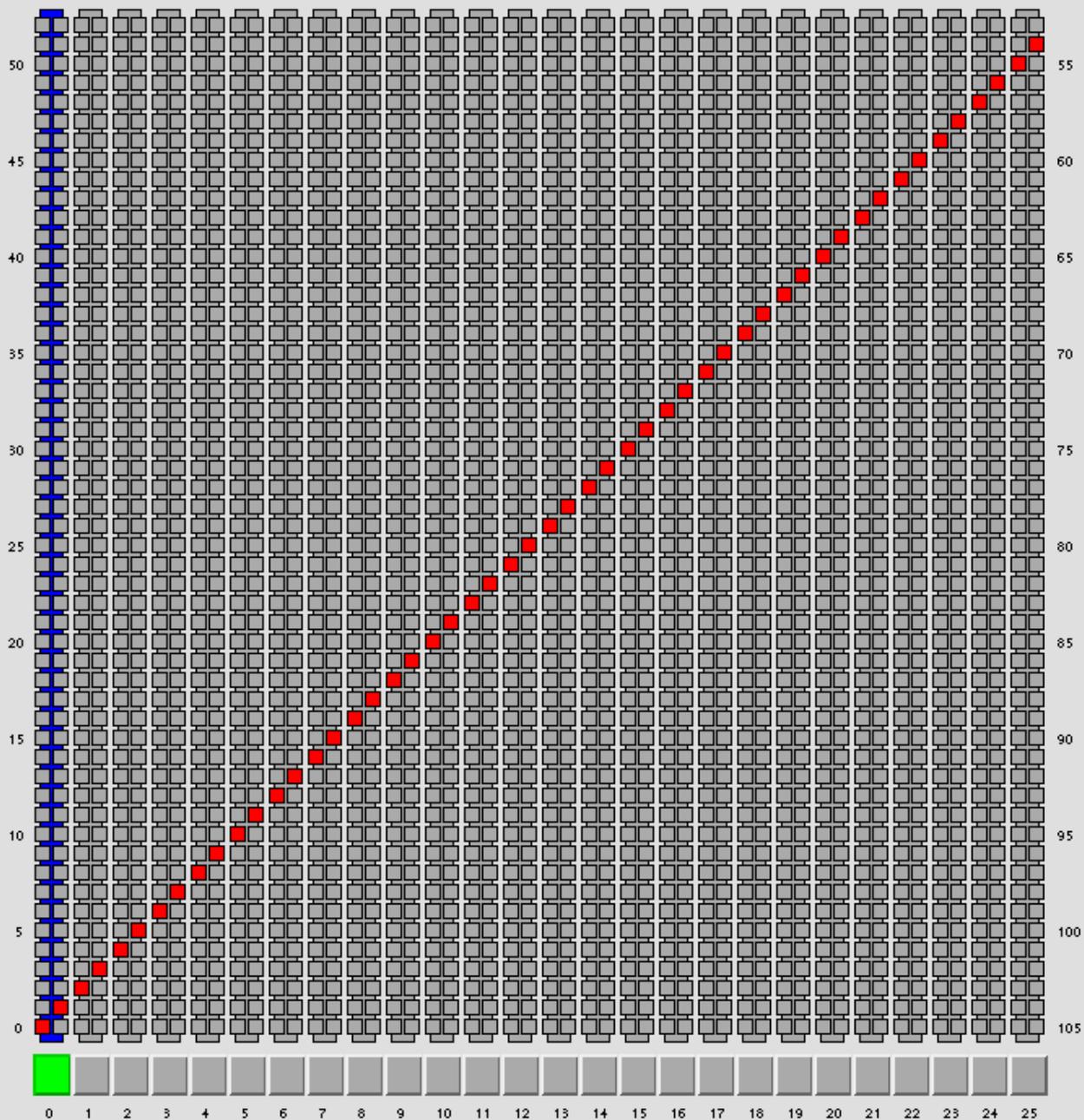
FPGA TBM at SiDet



# PSI43 Test Setups at FNAL

## Test software (Cosmo) from Rutgers

- Well designed Linux based GUI
- Point and click interface
- Provisions for DAC settings
- Runs on a Intel PC, Red Hat Linux 7.1
- Communicates with TBM via RS 232



# PSI43

## Chip Address Selection:

Hub:  Port:

Pixel (ROC) Chip:

## System Settings:

Readout speed:

Mode:

DAQ:

## Pixel Information:

Double- Column: 24

Column: 49

Row: 22

Trim: 4

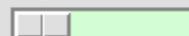
Calibrate: 0

Enabled: 0

## Pixel Write Change:

Trim Setting:

0



01234567

Calibration:

Pixel:

# K Pixel Chip DAC Settings

Set DAC defaults

Load DACs from file

Save DACs to file

## Supply:

Va- (V-)  
1.839

Vsf- (V-)  
3.33

Vc- (V-)  
2.055

vee- (V-)  
4.40

## Analog PUC:

VrgPr (V-)  
1.87

VrgSh (V-)  
2.15

VHidDel (V-)  
0.99

Vtrim (V-)  
1.23

## ReadOut:

VBias\_sf (uA)  
32.0

VOffsetOP (V-)  
2.47

VBiasOP (uA)  
60

VOffsetRO (V-)  
2.45

VIBiasAachen (uA)  
500

VOffsetCA (V-)  
3.50

VBiasAddr (uA)  
23.0

Vlon (uA)  
338

## Fast Trigger:

VIColOr (uA)  
450

VnPix (uA)  
350

VSumCol (uA)  
126.5

## Calibration:

VCal  
2.347

CalDel (ns)  
31.3

## Digital Register:

WBC (trigger latency):

14

+

-

Set WBC

Reset Inject

Set displayed DAC values



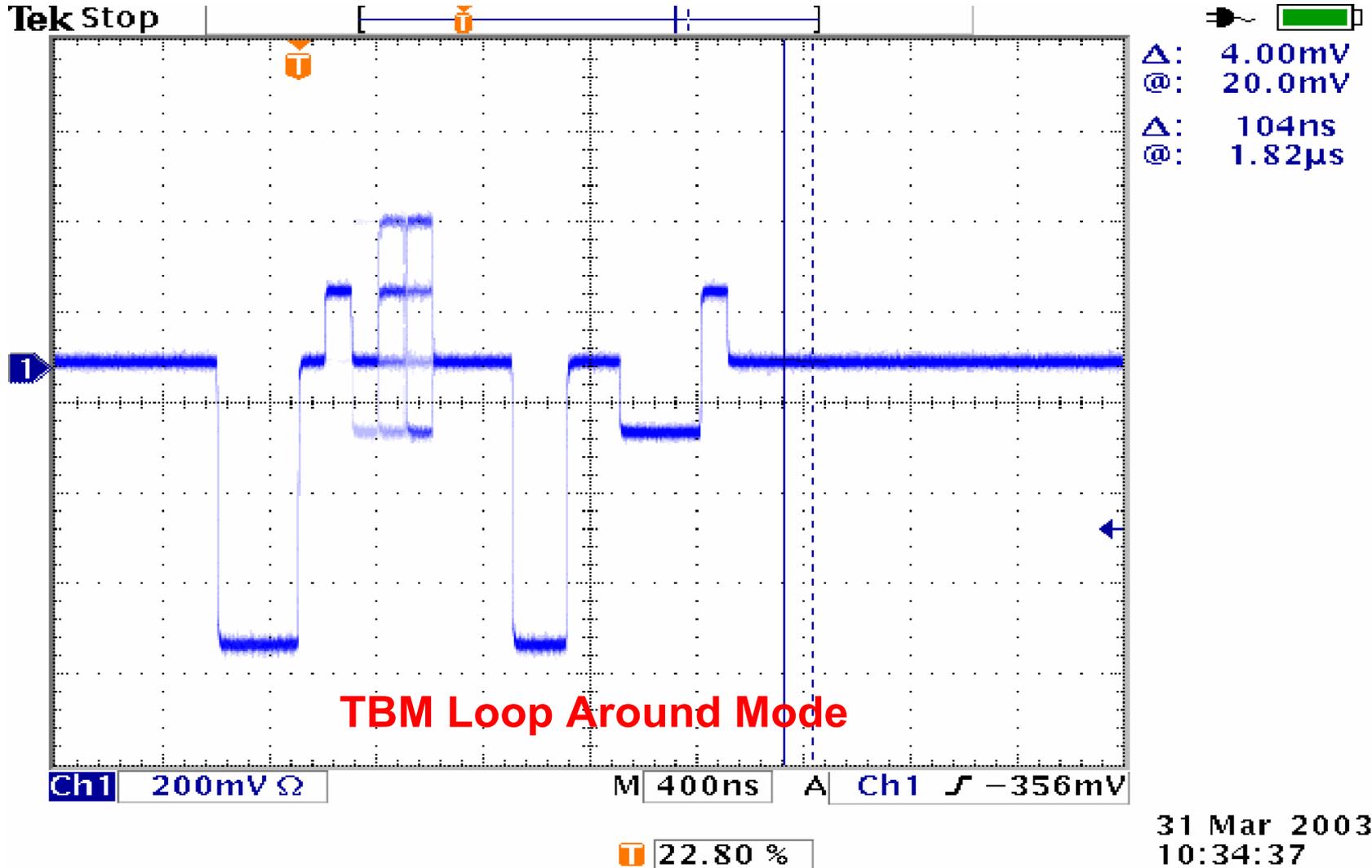
# PSI43 Test Setups at FNAL

## Procedure

- **Just started, still in learning mode**
- **Studied only 1 chip bonded to a VHDI and HDI**
  - Start with a chip designated “good” by probe tests (ASIC group).
  - Bond it to a VHDI (1x1) (@ FNAL SiDet)
  - Bond it to a HDI adapter board
  - Input clock 20 MHz & clock chip @ 20 MHz
  - Chip running @ 10 MHz



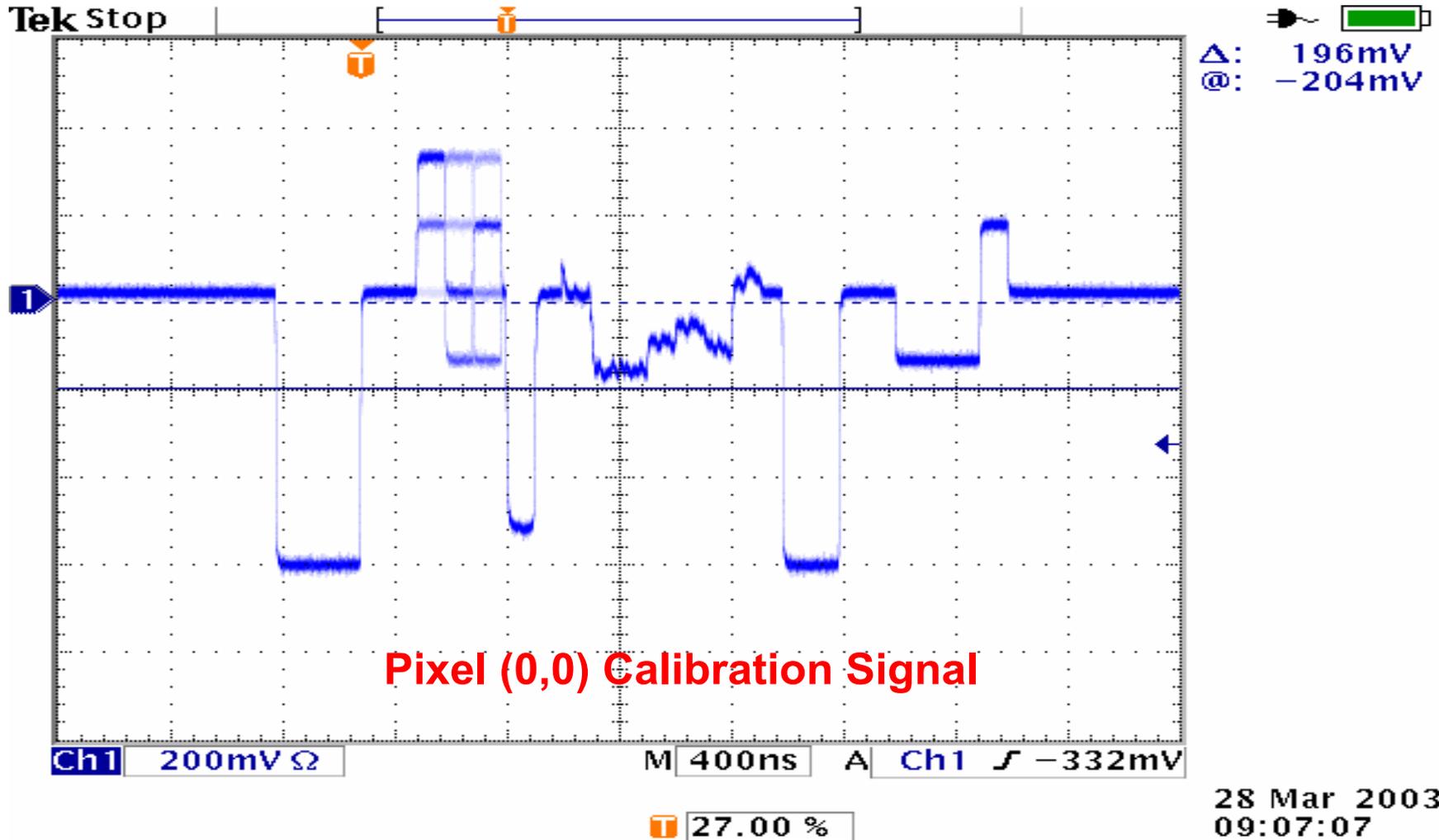
# PSI43 Test Setups at FNAL



31 Mar 2003  
10:34:37



# PSI43 Test Setups at FNAL





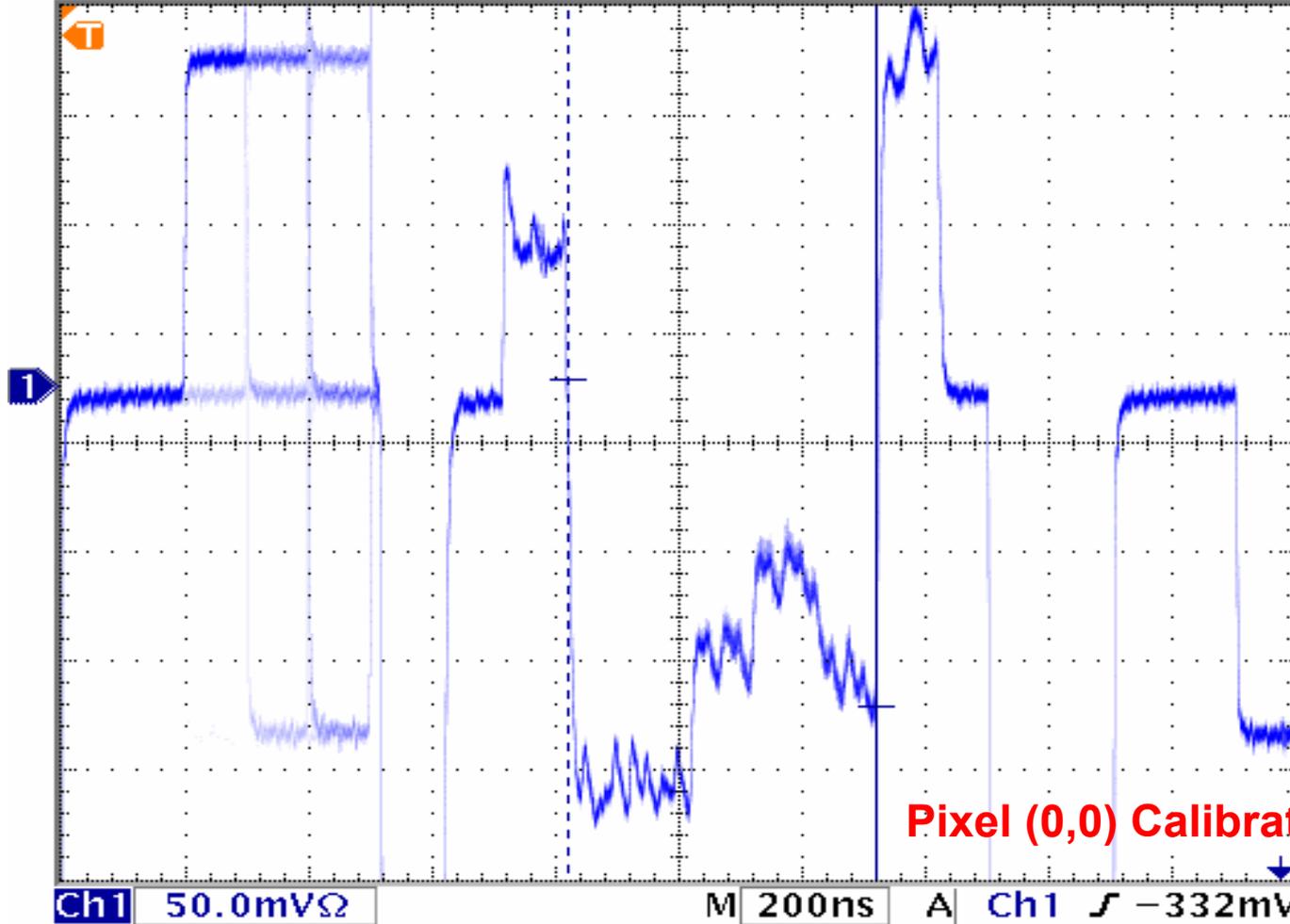
# PSI43 Test Setups at FNAL

- **Noticed a few things**
  - Signal very jittery. A 15 pF cap parallel to 1.6 M resistor (Boris)
  - Pickup in chip readout
  - Uneven row address '0' level ( $L_0$ )
- **Knew of no systematic method to set DACs**
- **Changed PUC DAC settings to maximize charge**



# PSI43 Test Setups at FNAL

Tek Stop



Δ: 150mV  
@: -147mV  
Δ: 500ns  
@: 1.32μs

Pixel (0,0) Calibration Signal

Ch1 50.0mVΩ M 200ns A Ch1 ⌘ -332mV

0.000 %

28 Mar 2003  
12:46:44

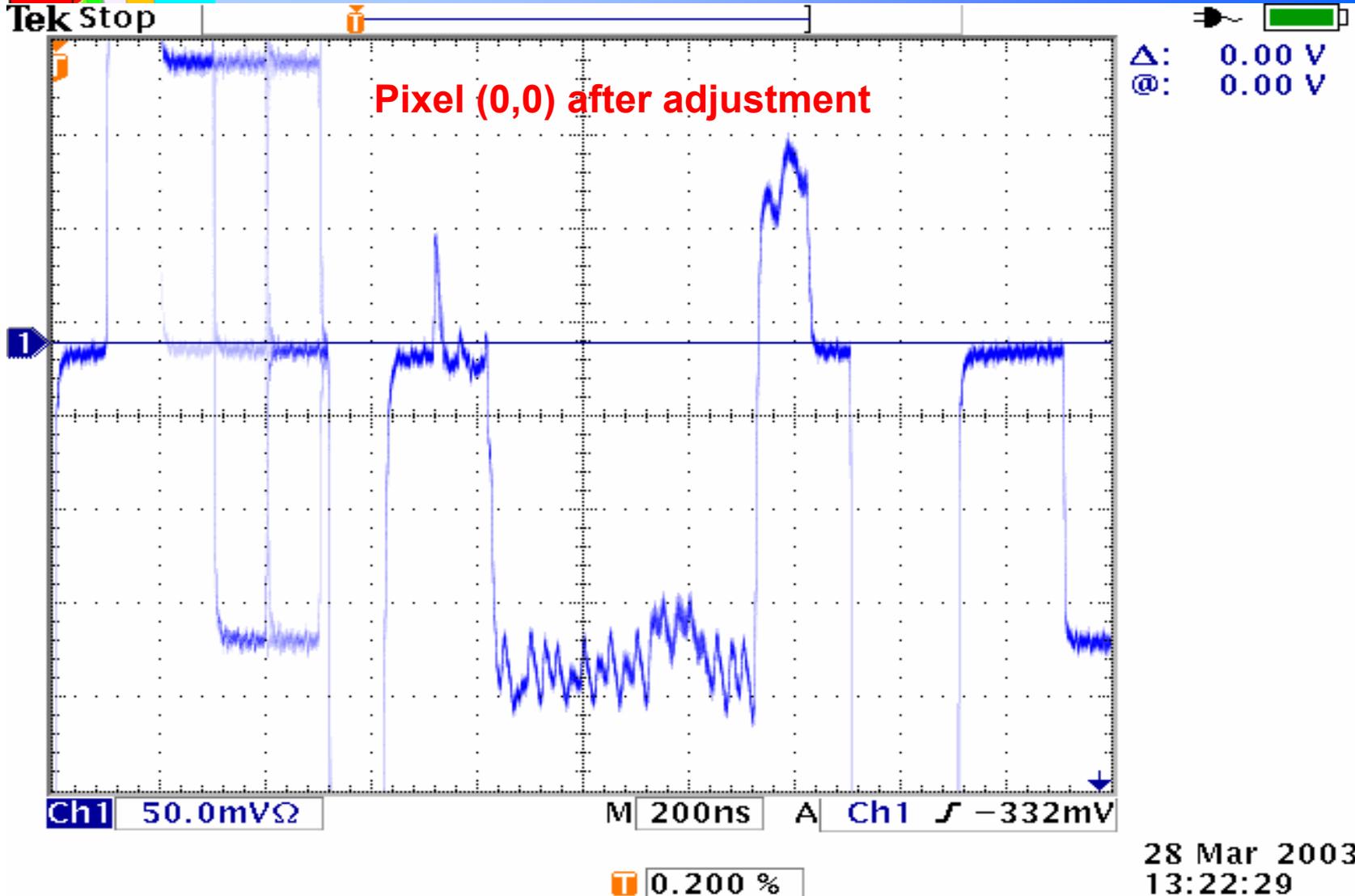


# PSI43 Test Setups at FNAL

- Step through individual pixels in **dc 0** to check various address signal levels
- Saw no change in row address  $A_1$  signal level in going from (0,15) to (0,20), i.e.  $L_3$  to  $L_4$ , and in  $A_2$  from (0,75) to (0,100), i.e.  $L_3$  to  $L_4$  **> Saturation**
- Adjusted  $V_{\text{offsetOP}}$
- Check various row address signal levels (5) within a double column – 5 different pixels



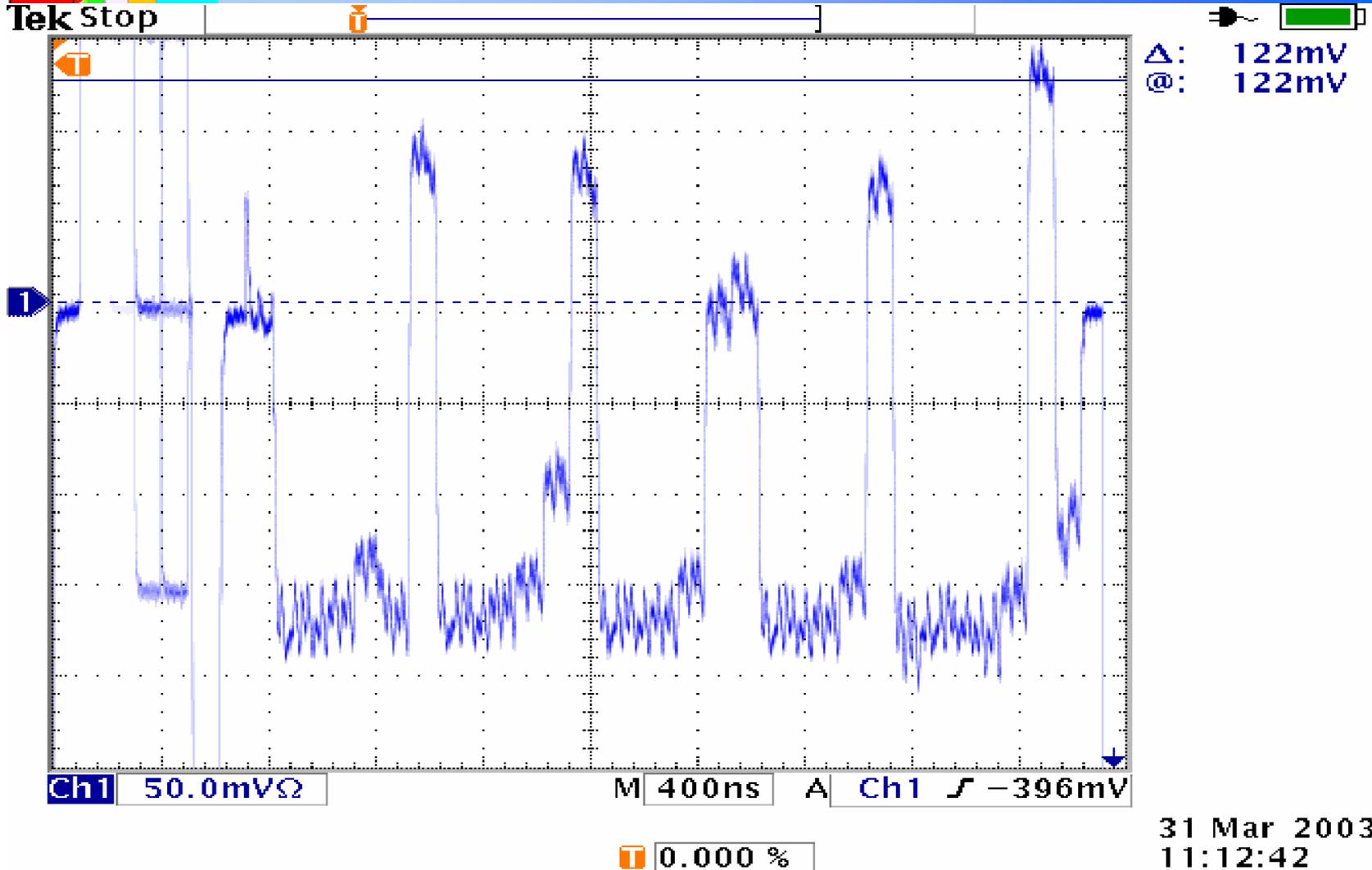
# PSI43 Test Setups at FNAL



28 Mar 2003  
13:22:29

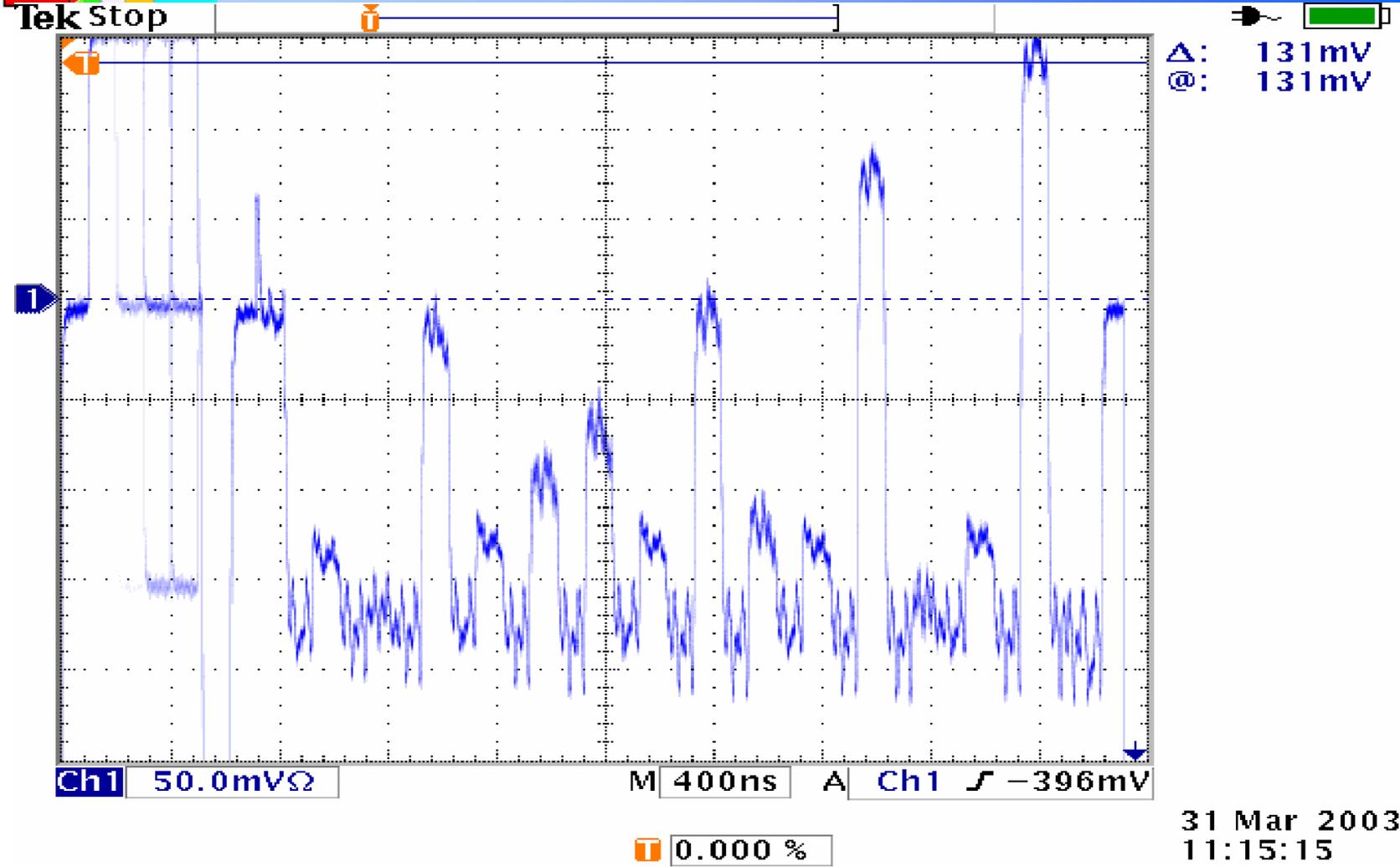


# PSI43 Test Setups at FNAL



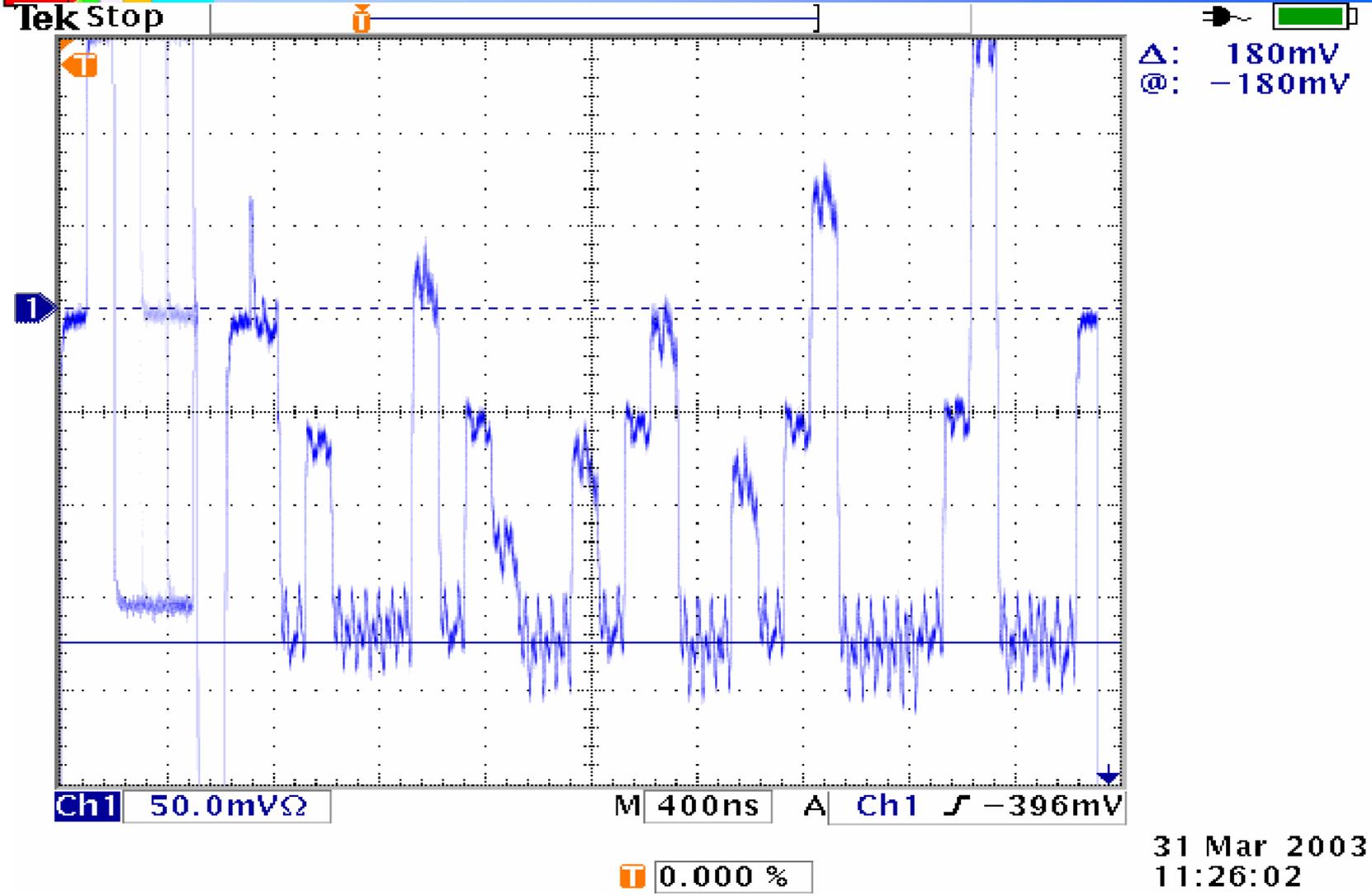


# PSI43 Test Setups at FNAL





# PSI43 Test Setups at FNAL





# PSI43 Test Setups at FNAL

- Repeat measurements but for different column addresses to check various column signal levels
- First for  $C_0$ , and then for  $C_1$



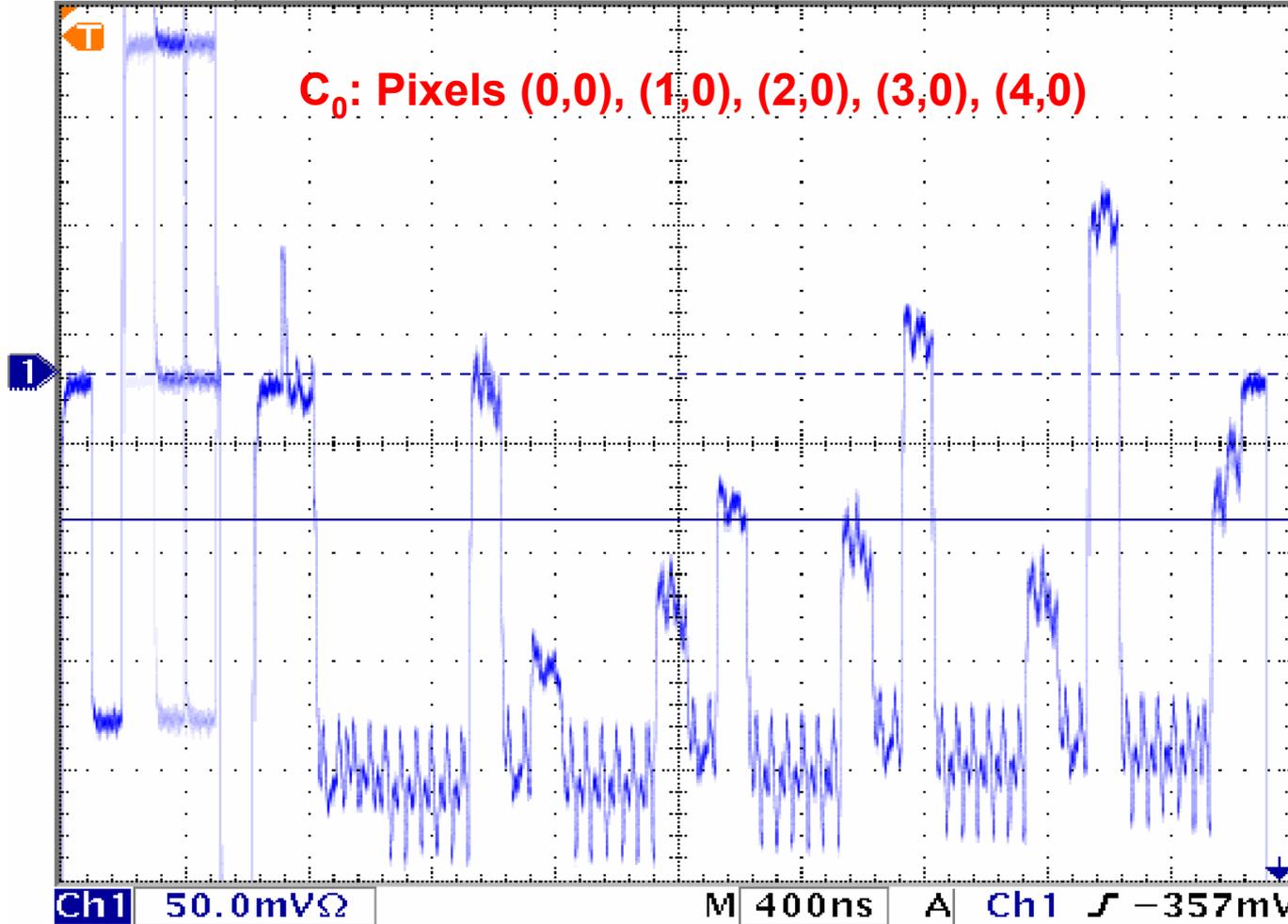
# PSI43 Test Setups at FNAL

Tek Stop



Δ: 67.0mV  
@: -68.0mV

$C_0$ : Pixels (0,0), (1,0), (2,0), (3,0), (4,0)



T 0.000 %

31 Mar 2003  
09:38:12



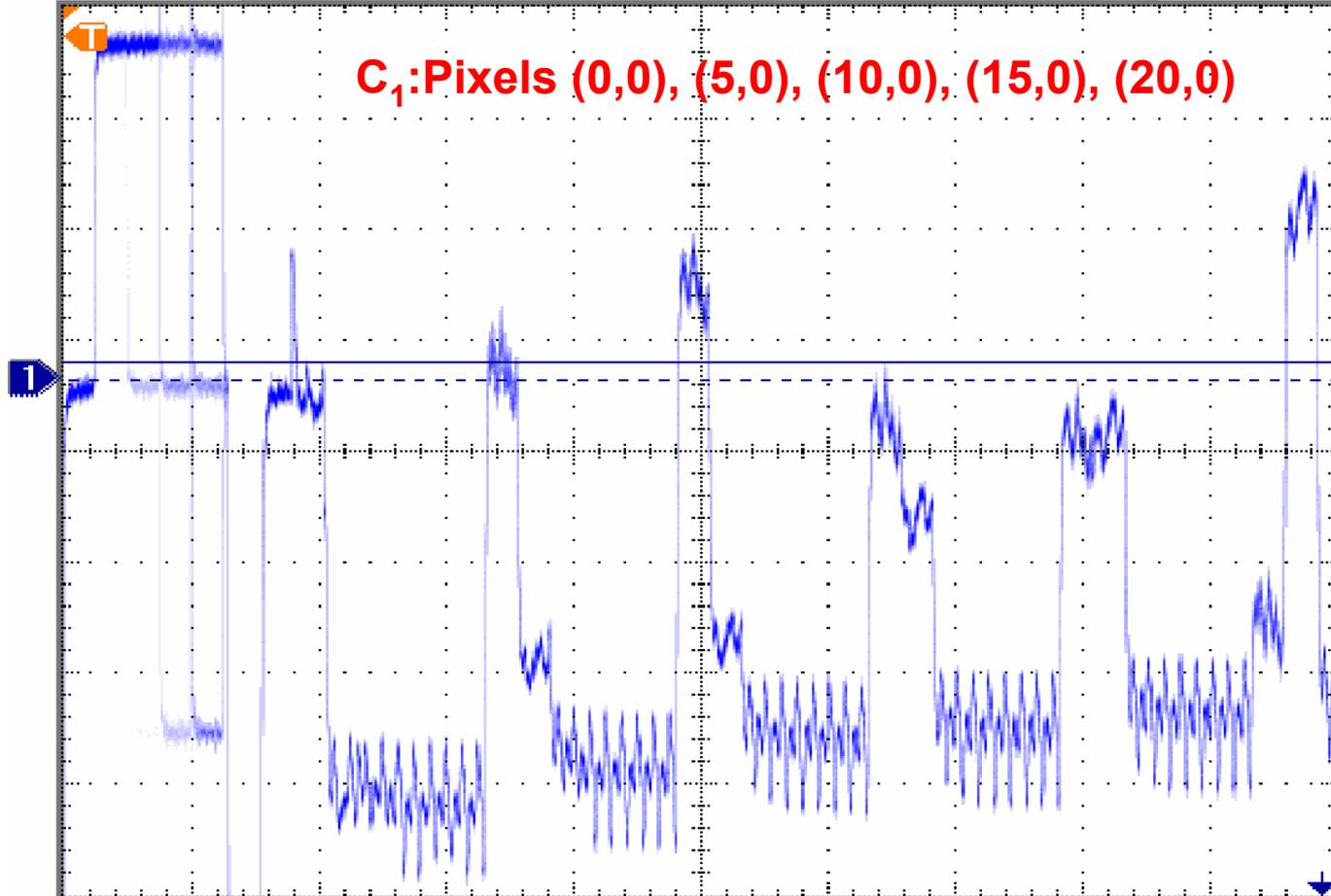
# PSI43 Test Setups at FNAL

Tek Stop



Δ: 8.00mV  
@: 7.00mV

C<sub>1</sub>: Pixels (0,0), (5,0), (10,0), (15,0), (20,0)



Ch1 50.0mVΩ

M 400ns

A Ch1 ∫ -357mV

T 0.000 %

31 Mar 2003  
09:46:08



# PSI43 Test Setups at FNAL

- Separation between levels  $L_1$  and  $L_2$  of column  $C_1$  very small  $\sim 10$  mV
- Found no DAC settings that widens the level separation
- The '0' levels of the addresses, both column and row, increase as higher levels are set in column  $C_1$
- **Perform more tests and understand them well**
- **Like to know of a systematic method to adjust DACs**
- **Prepare for  $0.25 \mu\text{m}$  ROC**