B.Baldin
C.Gingu
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ROC chip setup sequence

1. Load I2C FIFO with the following set of I2C commands:
   - Internal ROC registers

#	Device	DAC resolution	Address	Name	Default value	New value
1	DAC0	8 bit	0x04	Va-	61	211
2	DAC1	4 bit	0x05	Vsf-	11	1
3	DAC2	8 bit	0x06	Vc-	65	193
4	DAC3	4 bit	0x07	Vee	4	2
5	DAC4	8 bit	0x08	VrgPr	130	92
6	DAC5	8 bit	0x09	VrgSh	149	92
7	DAC6	8 bit	0x0A	VHldDel	65	130
8	DAC7	4 bit	0x0B	Vtrim	8	13
9	DAC8	4 bit	0x10	VBias_sf	6	9
10	DAC9	4 bit	0x11	VOffsetOP	11	3
11	DAC10	4 bit	0x12	VBiasOP	7	7
12	DAC11	4 bit	0x13	VOffsetRO	5	9
13	DAC12	4 bit	0x20	VIBiasAachen	10	15
14	DAC13	4 bit	0x21	VOffsetCA	15	1
16	DAC14	4 bit	0x22	VBiasAddr	7	7
17	DAC15	4 bit	0x23	Vion	6	14
18	DAC16	4 bit	0x40	VIColOr	15	10
19	DAC17	8 bit	0x41	VnPix	36	0
20	DAC18	8 bit	0x42	VSumCol	254	112
21	DAC19	8 bit	0x80	VCal	187	100
22	DAC20	8 bit	0x81	CalDel	0	64
23	WBC	-	0x82	Trigger Latency	25	25
24	CTRL	-	0x83	Control register	0x03	3

- Pixel setup data

Set all pixels to a masked state with trim bits set to 4 by repeating the following set of I2C commands (binary):

10100100, 1ccccccc, 0ppppppp, 01000000,

where, ccccccc – column address in Gray code (0…51)

pppppppp – row

address in Gray code (0..52).

Disable all double column peripheries by repeating the following set of I2C commands (binary):

10100100, 1ddddddd, 00100000, 00000000,

where, dddddddd – double column address in Gray code (0..50, step 2).

Insert I2C Stop after each command by using 9th FIFO bit.

2. Setup ROC internal registers by issuing "Start I2C command stream".
3. Check FIFO empty status flag to verify that FIFO command stream is exhausted.
4. Issue PSI43 timing reset by pulsing PO11.
5. Enable "sequencer on" bit.
6. At this point we should be ready to see ROC analog output on the scope.