ASIC Review Committee Report

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A review of the activities of the Fermilab ASIC group was presented on December 12, 2011. This is the report of the review committee.

Findings

Analog and mixed mode IC design has been, and continues to be, the core strength of the ASIC group. The development of the QIE10, the NOvAchip, and the FPHX chip are excellent examples of this strength. The proposed CMS pixel upgrade project also appears to be well aligned with the strengths of the group.

Fermilab has played a leadership role in exploring the use of 3D IC technology for HEP. This line of R&D was motivated primarily by the needs of an ILC vertex detector and has been a focus of the ASIC group for a number of years. The group provided an important service for the worldwide HEP community as the organizer of the 3DIC Consortium. One measure of the success of this effort is the decision by CMP/CMC/MOSIS to take over from Fermilab the job of organizing MPW wafer submissions to Tezzaron/Chartered.

The Vertically Integrated CMS Tracker (VICTR) effort was started based on experience gained in ILC motivated 3D R&D. As currently envisioned, VICTR incorporates essentially all of the 3D integration techniques that the group has explored, but the design concept is flexible enough so that it could succeed even if some of the technologies are not included in the final product. This project could have a large beneficial impact on the capabilities of CMS in the HL-LHC era.

The ASIC group has also been pursuing the development of monolithic SOI detectors (mostly in the context of the SOIPIX collaboration led by KEK). This R&D was also motivated primarily by the needs of an ILC vertex detector. Although the effort devoted to SOI design has been small compared to the 3D effort, the ASIC group has made significant contributions to SOIPIX.

The work of the ASIC group has been largely consistent with the mission of Fermilab and the field. With respect to future Intensity Frontier experiments, ASIC R&D needs have not yet been articulated by these initiatives.

The model presented for access to the resources of the ASIC group is based on bi-lateral and often ad-hoc communication between engineers and customers (usually scientists). No process or model of assigning priorities was presented.

A significant fraction of the M&S budget of the ASIC group is devoted to software licenses. The group works hard to minimize these costs, but the pricing model of the single supplier (Cadance) of most of the software ensures that the cost to FNAL is much higher than the cost of the same software for a university group.

Comments

The presentation of Fermilab's ASIC R&D effort should follow an appropriate hierarchical decomposition, starting with a "big picture" overview, and drilling down into topics, sub-(sub-) topics, and details."

It would be valuable to understand and capture what the USHEP ASIC portfolio is/should-be, which is the first step in understanding Fermilab's role in the portfolio.

To the extent that Fermilab can frame the discussion and debate in the forthcoming detector R&D (KA15) review, the focus should not be on a value analysis but rather where the Fermilab team can excel and lead in the USHEP ASIC portfolio.

3D IC technology remains high risk, but has really revolutionary potential for HEP. This line of R&D should remain part of Fermilab's portfolio.

While the value of ad-hoc and informal communication between Fermilab engineers and scientists should not be underestimated, the question of how access to the ASIC group and group priorities are managed does not currently have an impressive answer.

Management should be alert to opportunities that arise for the ASIC group to contribute significantly to Intensity Frontier experiments.

Regarding lab-wide integration, the ASIC team is reasonably well integrated with allied EE efforts in PPD and the Scientific Computing Division. The awareness of and integration with lab-wide engineering initiatives such as Team Center should be improved.

The ASIC group has relatively modest requirements with respect to test and measurement equipment, but relies on rather expensive software. The software costs are unlikely to decrease with time and may increase substantially as the group begins to design more complex ICs using advanced CMOS processes. These costs are unavoidable if Fermilab is to have an ASIC design group.

Some level of non-HEP projects is valuable because it broadens the experience base of the ASIC engineers and provides interesting work when the HEP related demand is low. The case for these projects is easiest to make if they are largely supported by work-for-others agreements and other external funding arrangements.

Consideration should be given to the establishment of joint Fermilab/University EE staff appointments (similar to the existing joint Scientist appointments). This could provide more direct access for student participation in R&D projects and possibly access to lower cost CAE and CAD tools.