

# Readout for SiPMs

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2/17/2009

# SiPMs readout for ?



- ▶ Define area of application
  - They are not **Die eierlegende Woll-Milch-Sau**

R. Mirzoyan

(approximate english translation: all-in-one device suitable for every purpose)

I will only address **READOUT** of device that are  
moderate area (up to 5 x 5 mm )  
moderate pixel count ( up to  $10^5$  pixel )  
moderate speed (up to 1 ns resolution)

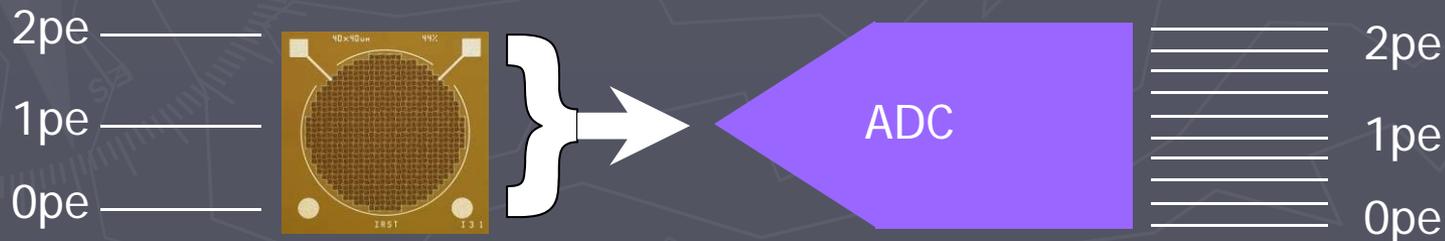
for HEP applications

# The Future



## ► I have seen the future of SiPM readout

- Readout electronics **will be integrated into the SiPM!** because
  - SiPM is an inherently digital device
  - We **ALWAYS** convert the signal from the SiPM to digital
  - So why do we have an analog step in between?!?



# The Future



## ► Ingredients required for integrated readout

1. SiPM is CMOS compatible

RMD makes SiPMs through Mosis



2. Will work for in HEP applications

Pixel architectures have demonstrated readout of arrays like this



3. Cost effective  
(in volume)



# So why DIGITAL-ANALOG-DIGITAL?

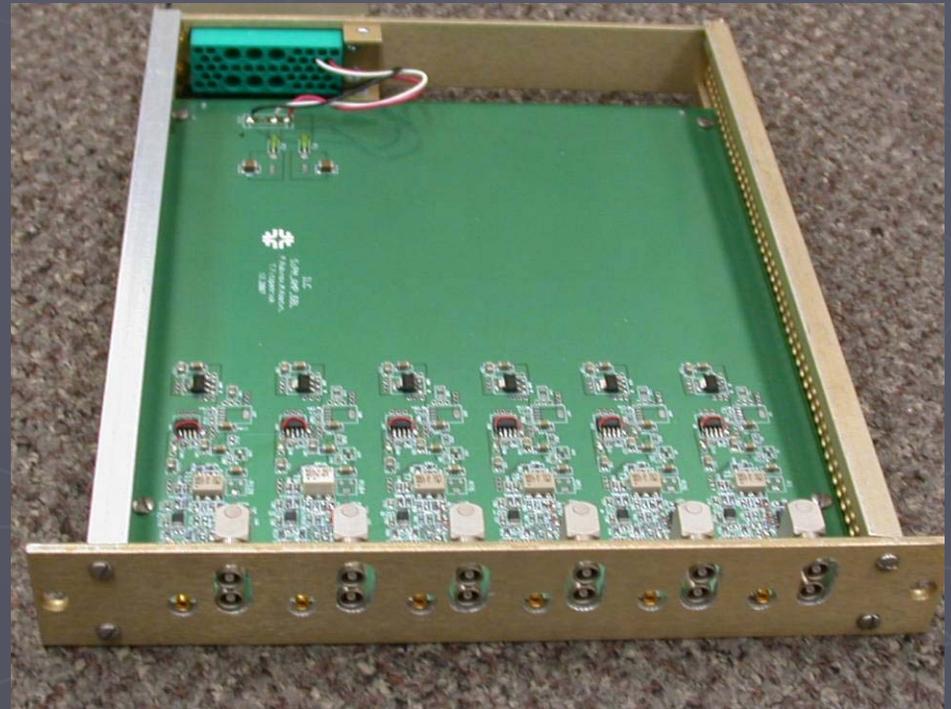
- ▶ Because this requires an ASIC
  - The people who make SiPMs do not know what we want
  - The people who know what we want do not make SiPMs (yet)

Application Specific IC has to have a specific application

Because it gives us the most flexibility

# Back from the future

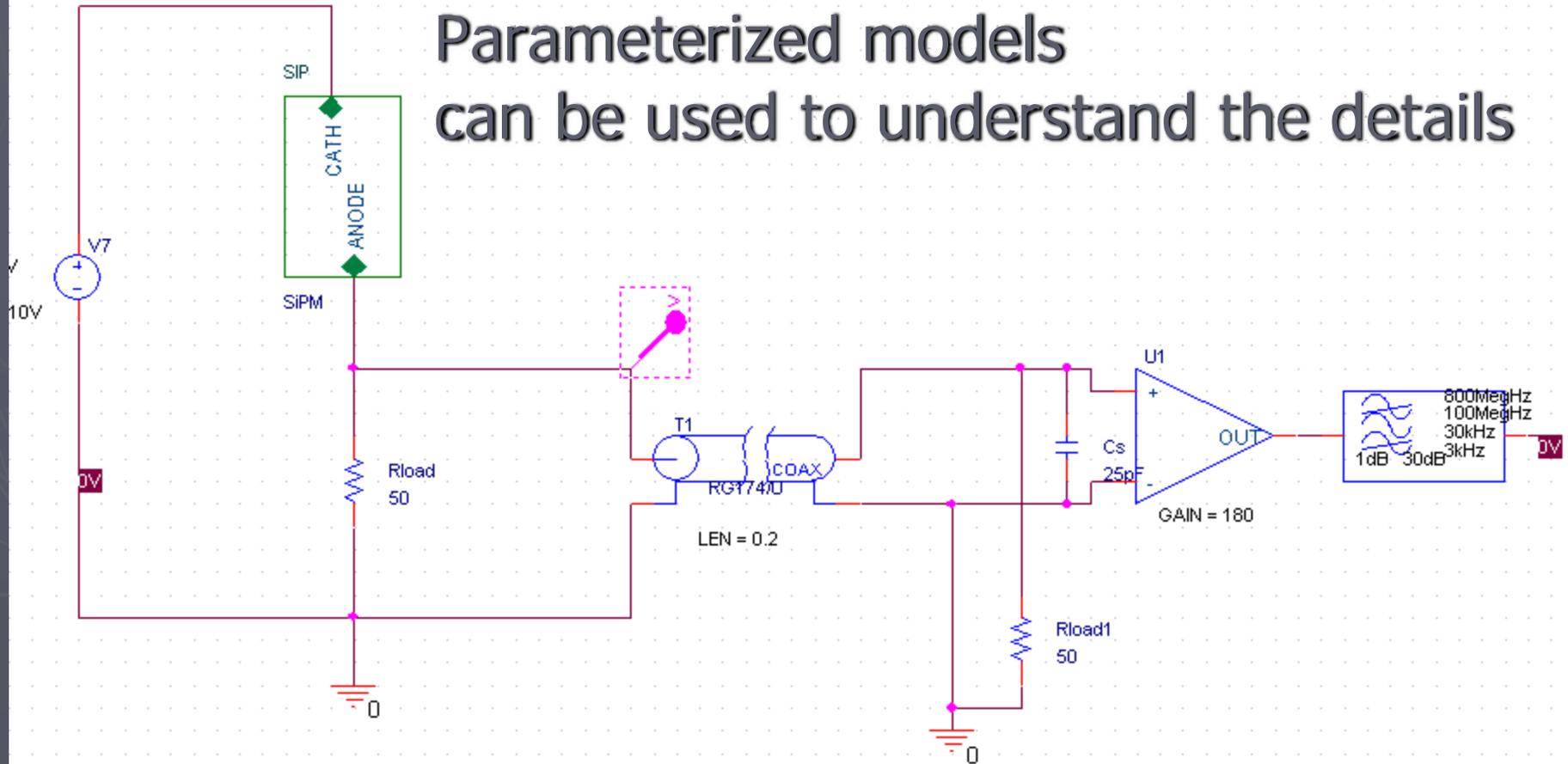
- ▶ Our current strategy is to maximize flexibility
  - which is the opposite of what we eventually want

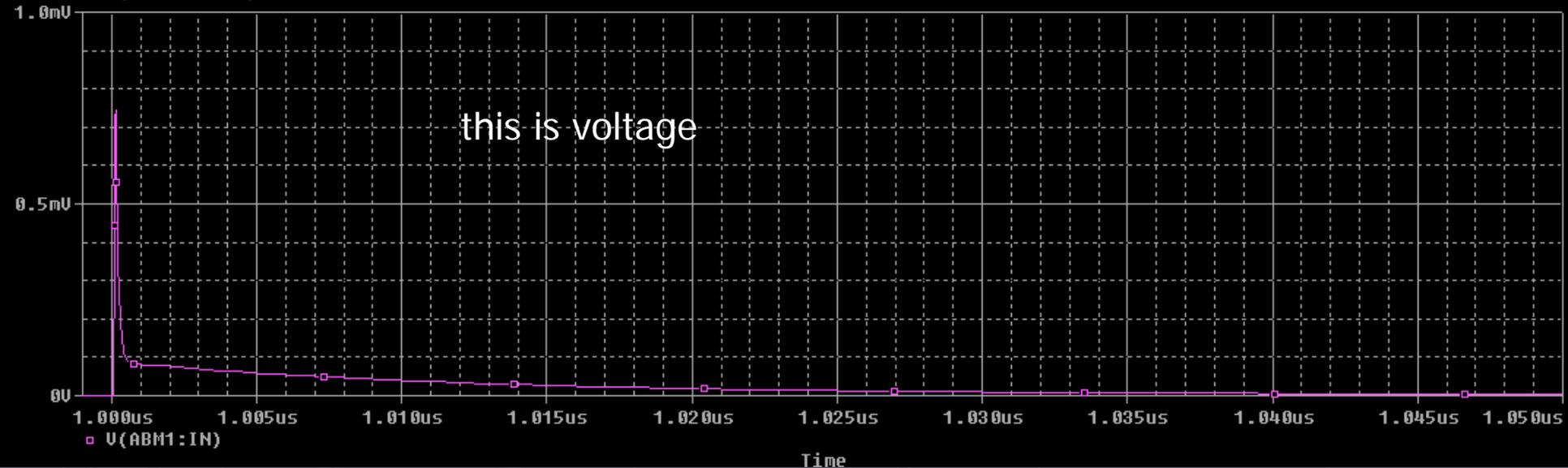
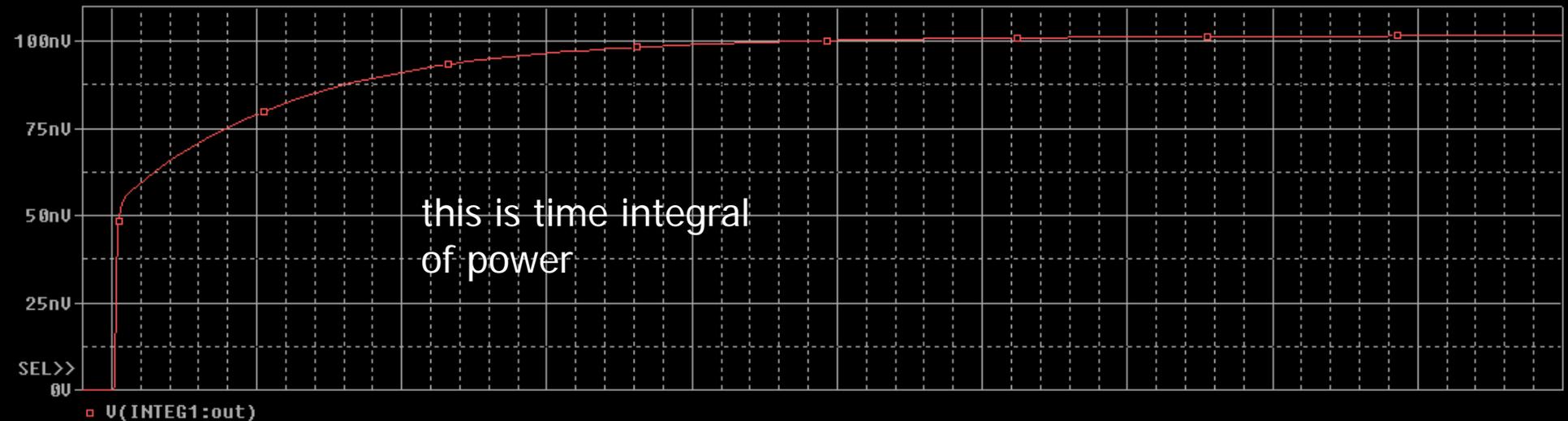




# Simulating SiPM

Parameterized models can be used to understand the details

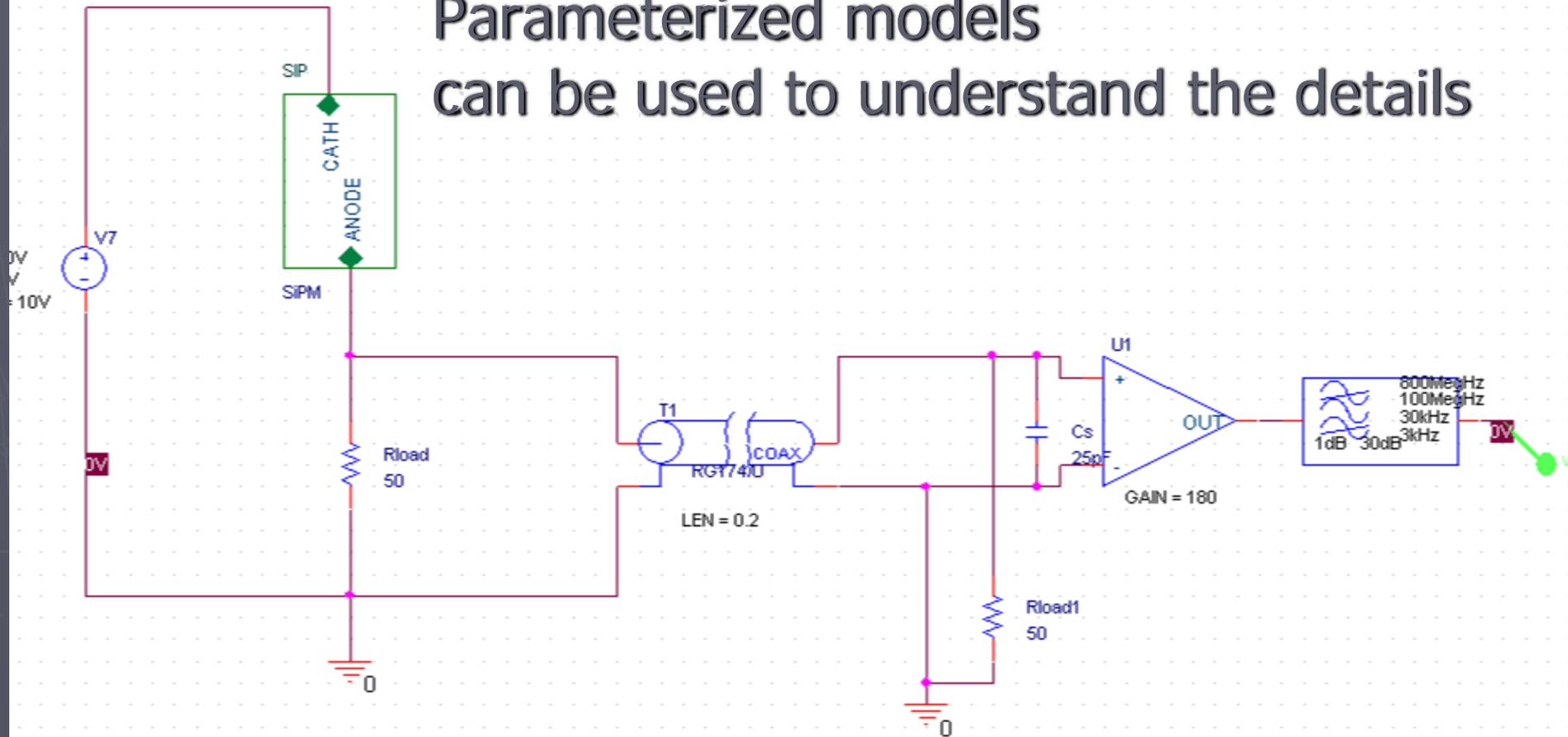




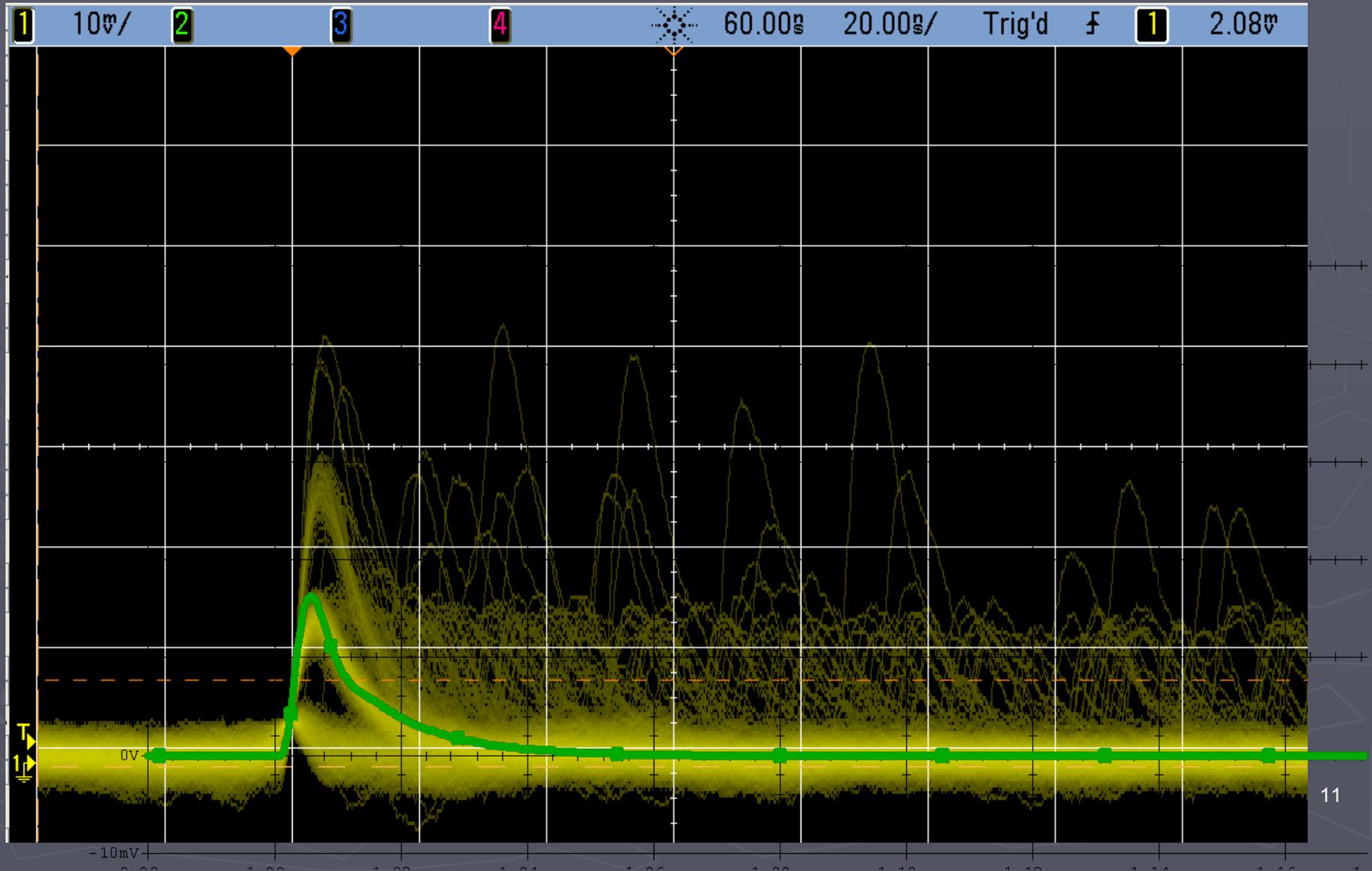
- ▶ It depends on  $C_{rp}$ , but a reasonable guess is that about half the energy is in the spike and half in the "slow" part
- ▶ Studies of temperature dep can be used to understand

# Simulating SiPM

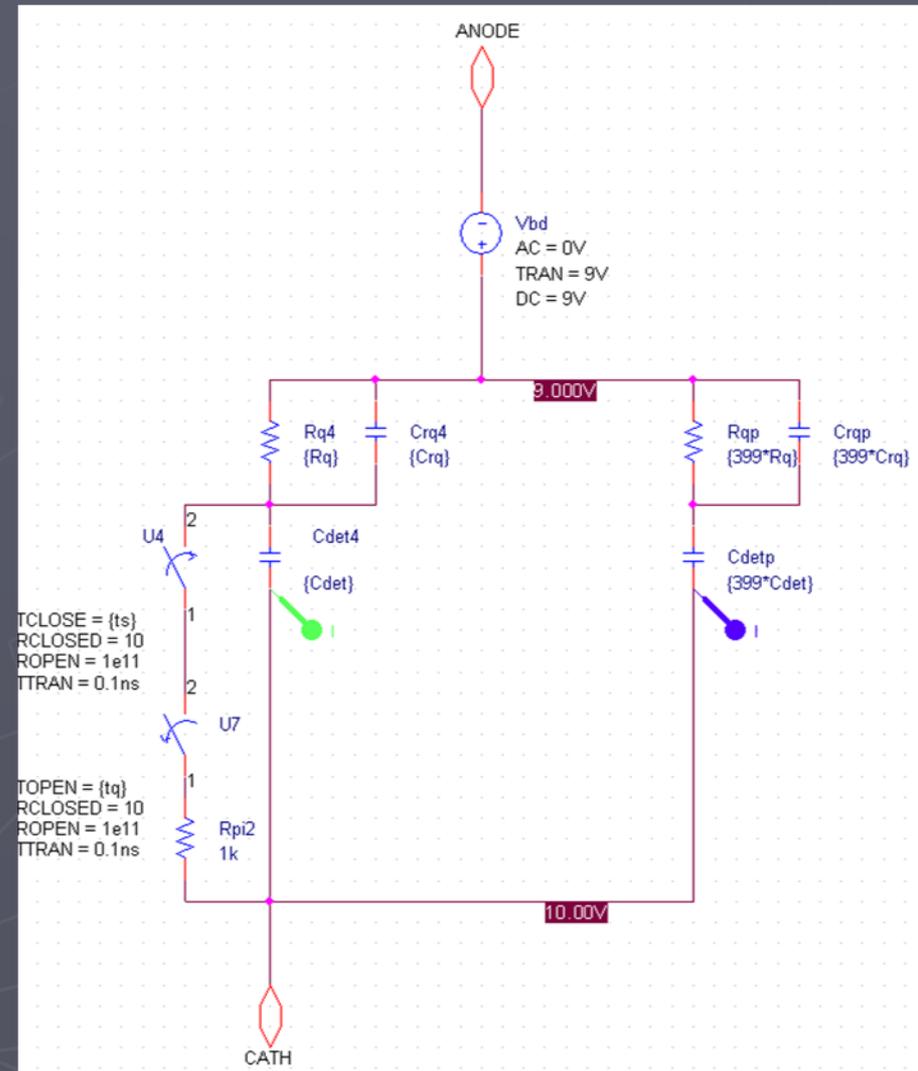
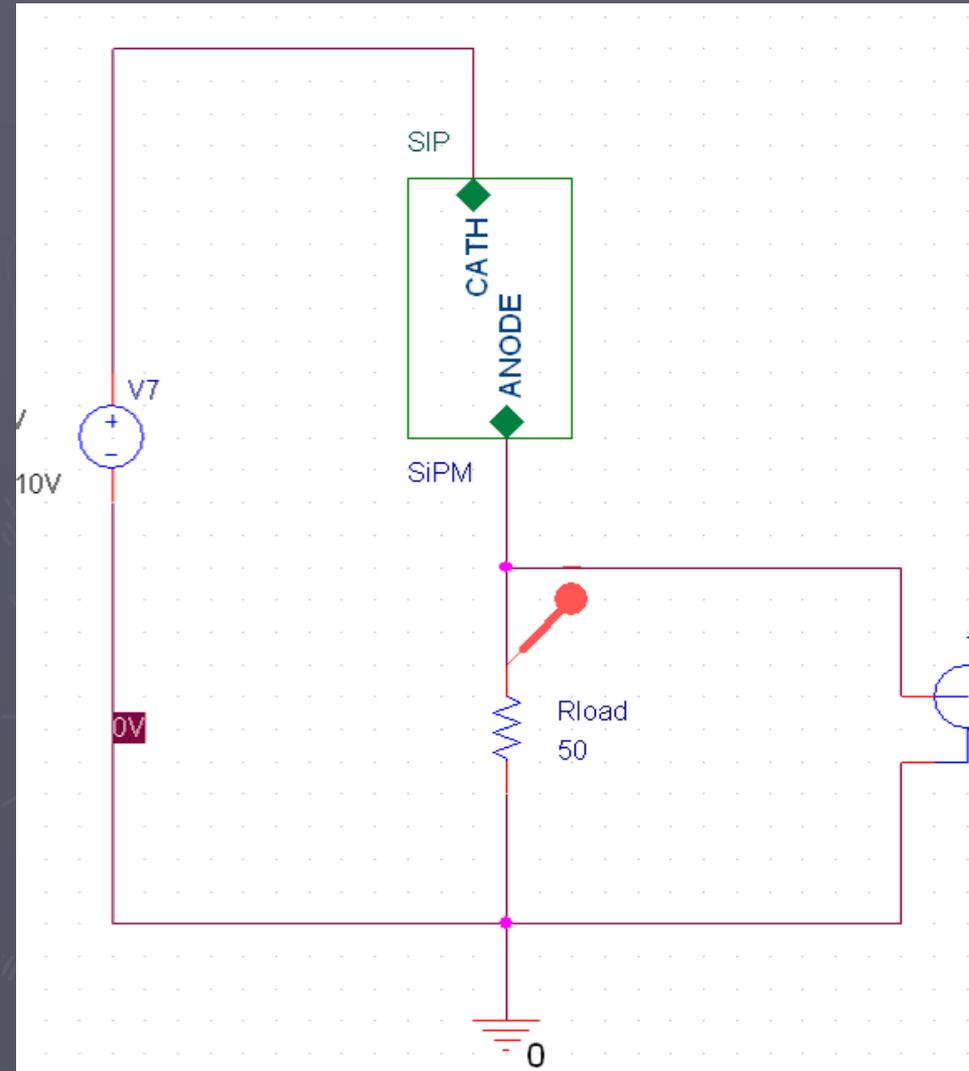
Parameterized models can be used to understand the details



# Simulation vs reality

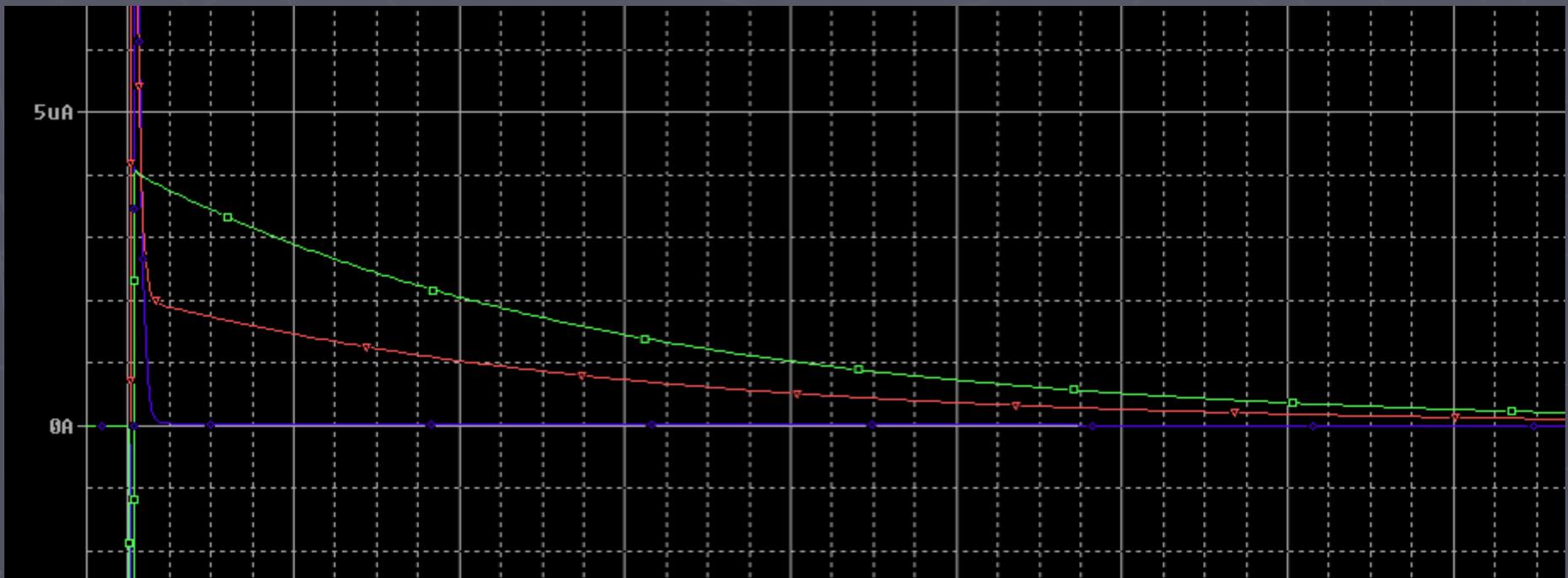


# Can be used to look "inside"



# Can be used to look "inside"

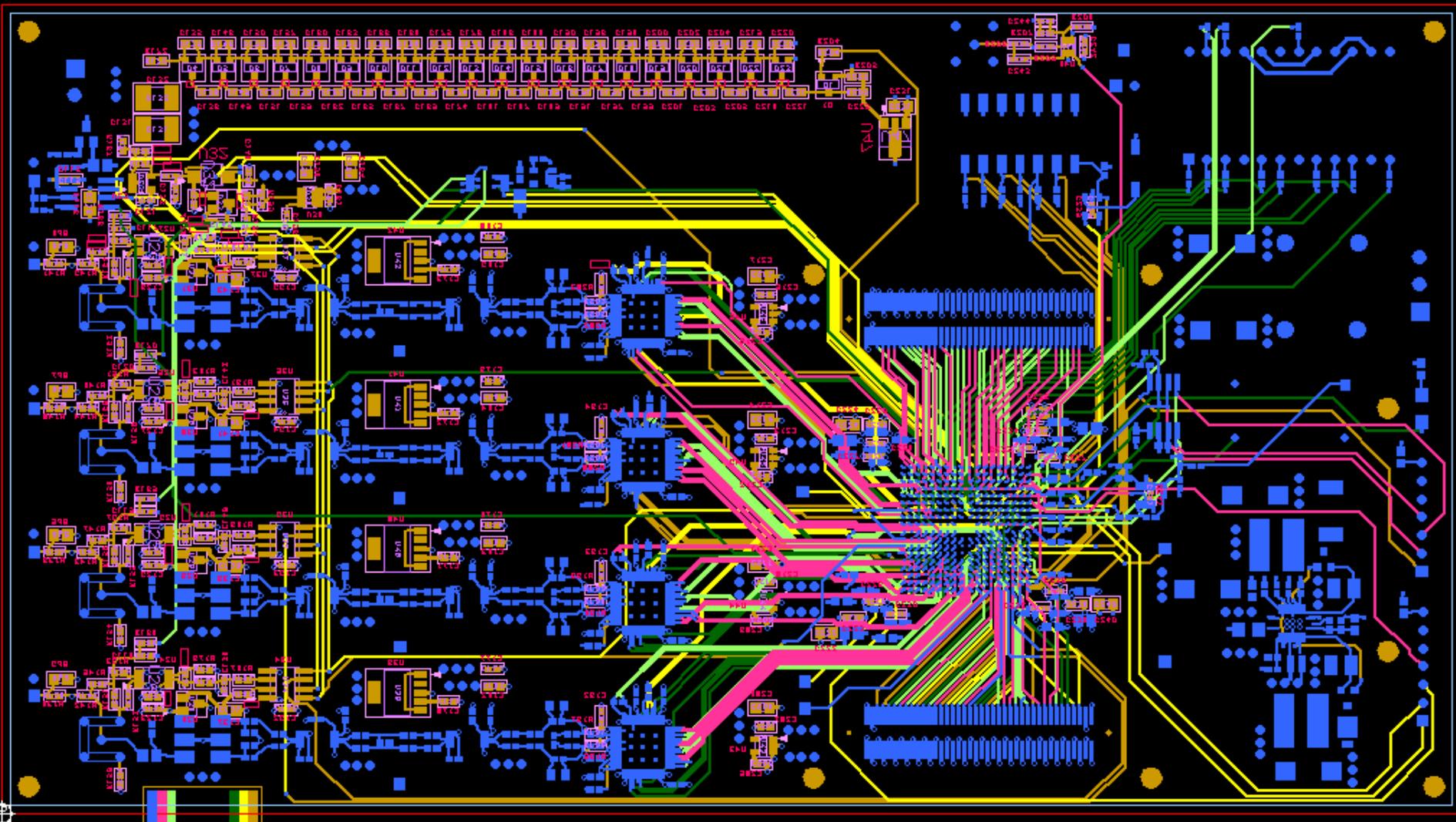
So we see that the **output signal** is a **slow recharge** of the cell capacitance and a **fast spike** through the grid capacitance



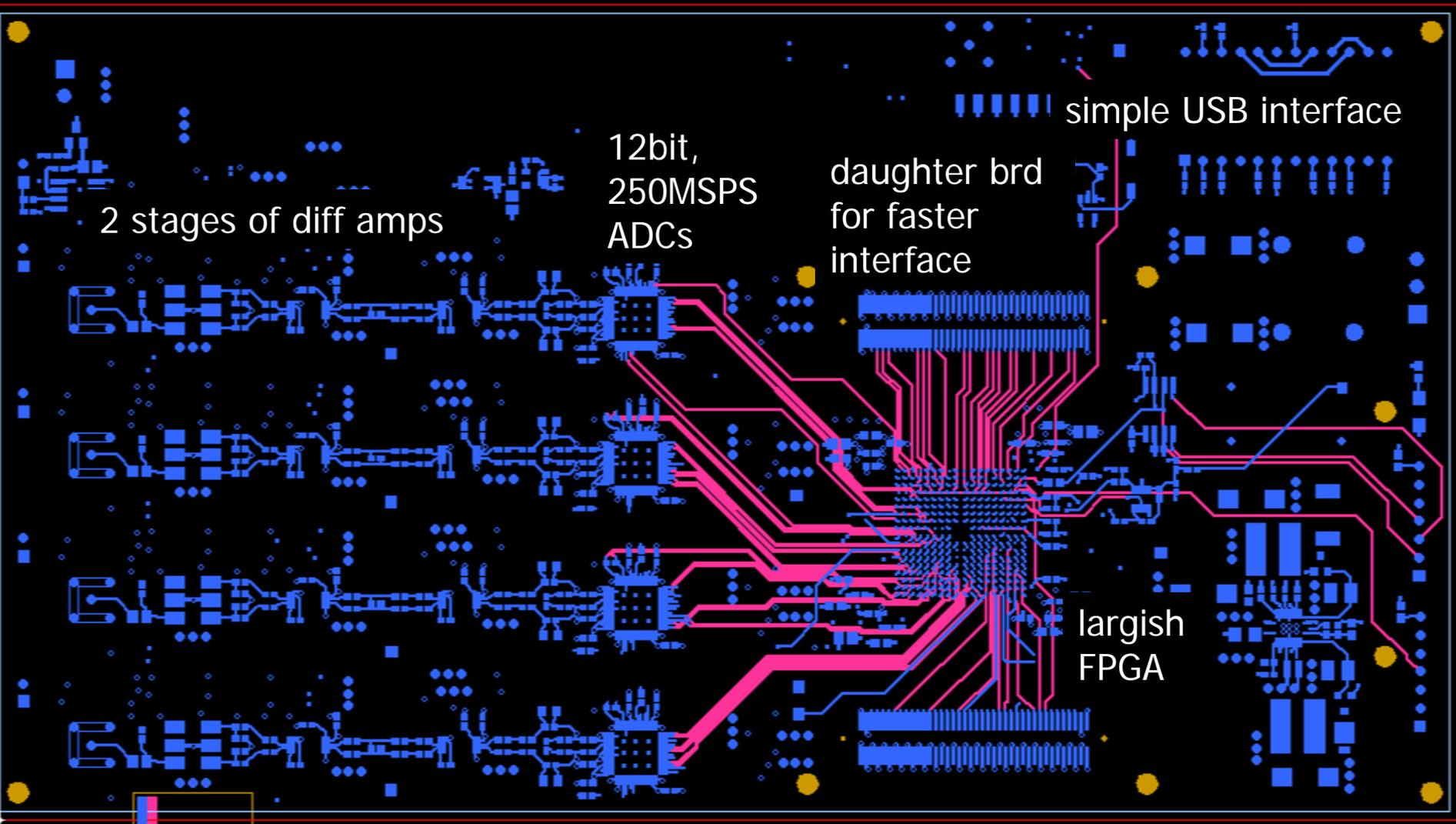
# Next step(s): 4ch board

- ▶ Still very generic, but now think infrastructure
- ▶ Best available commercial components without heroic efforts ( $\sim 1\text{ns}$  resolution,  $\sim 400$  pe range)
- ▶ Integrated with SiPM specific features (bias generator, current readback, temp sensor)
- ▶ Optimized for medium ch count (dozen(s) SiPMs)
- ▶ Flexible: using 50ohm input, generic daughter board connection to support faster readout/more memory
- ▶ Large FPGA to allow DSP and TDC features

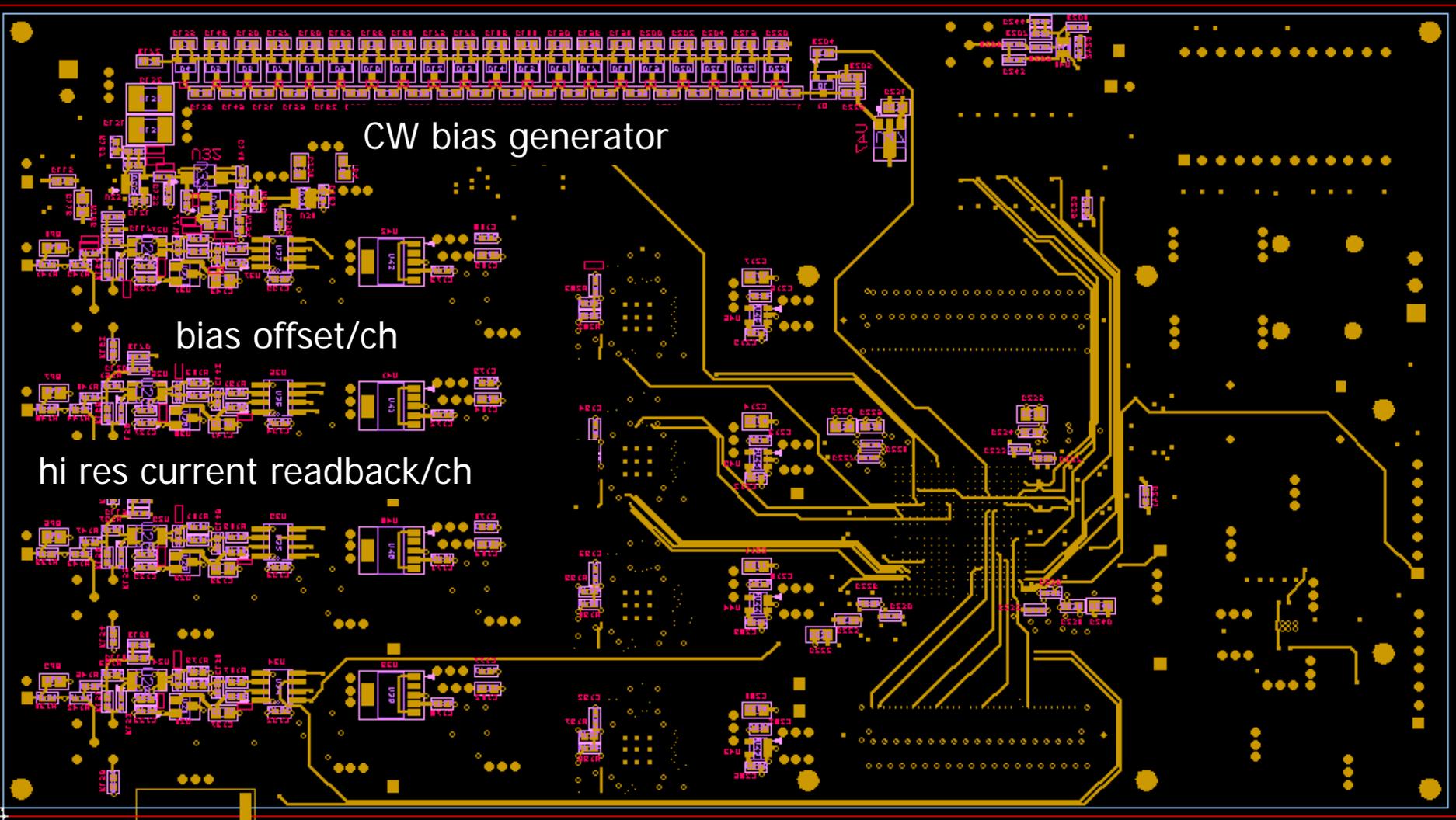
# Next step(s)



► Still very generic, but now think infrastructure



► Still very generic, but now think infrastructure



# Near future

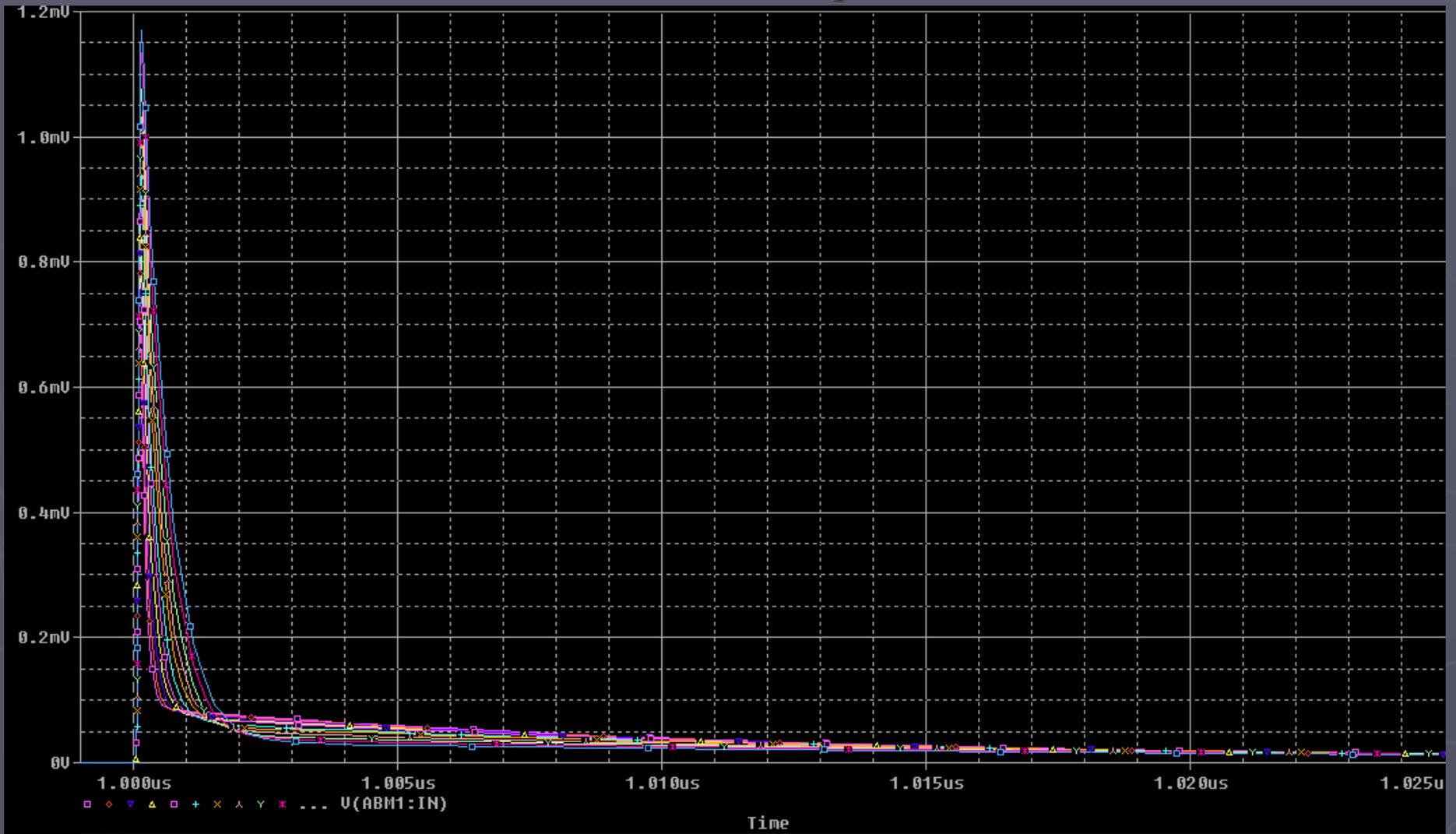
- ▶ Move from more generic to more specific
- ▶ Become tied to mechanics  
(drop long 50ohm cables)
- ▶ Specific for:
  - larger volume testing
  - larger (specific) detector application
- ▶ Optimize for 100s of SiPMs

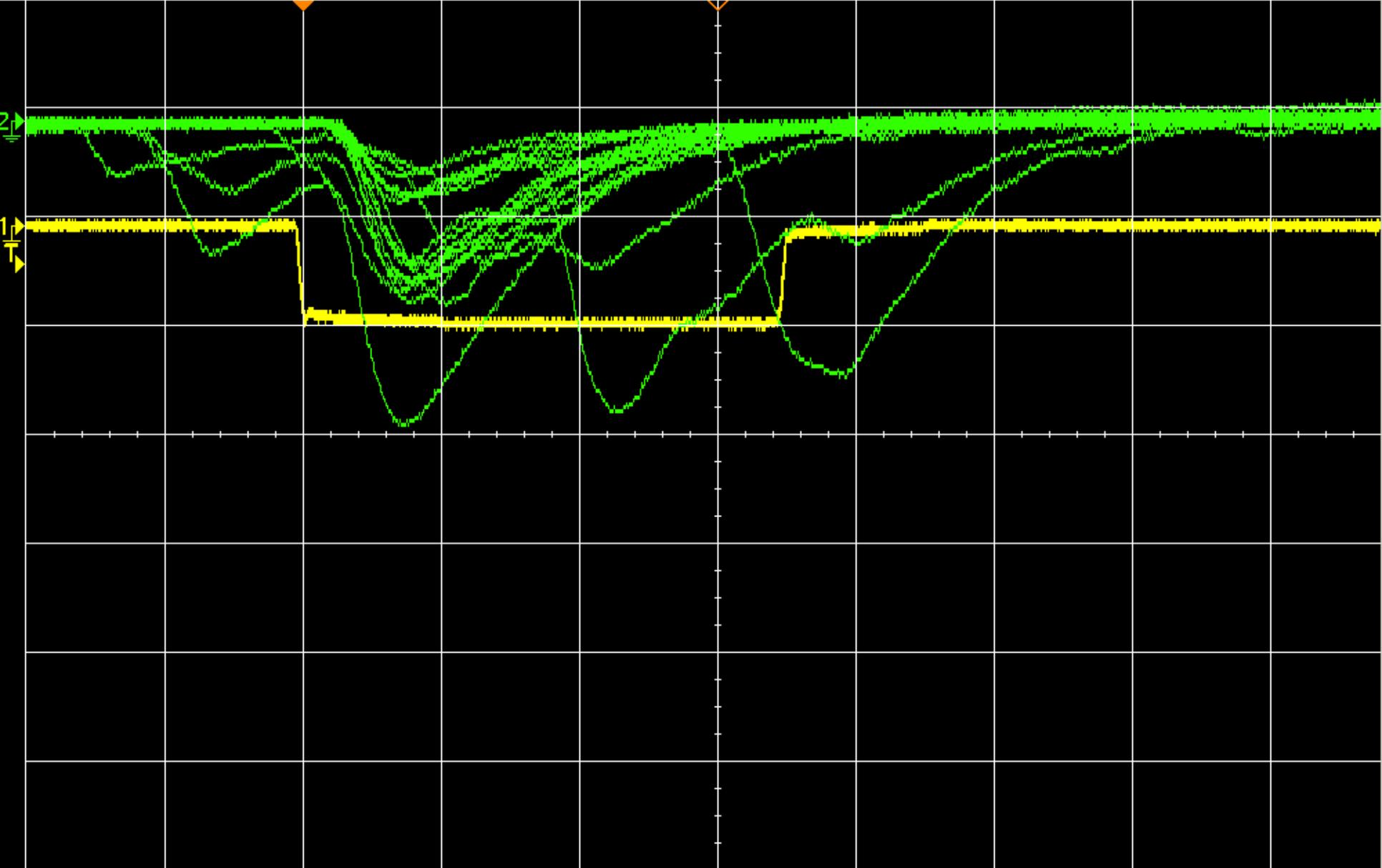
# Conclusion

- ▶ I think the way forward is clear
- ▶ To take full advantage of SiPMs, there must be an ASIC
- ▶ If we don't do this, others will

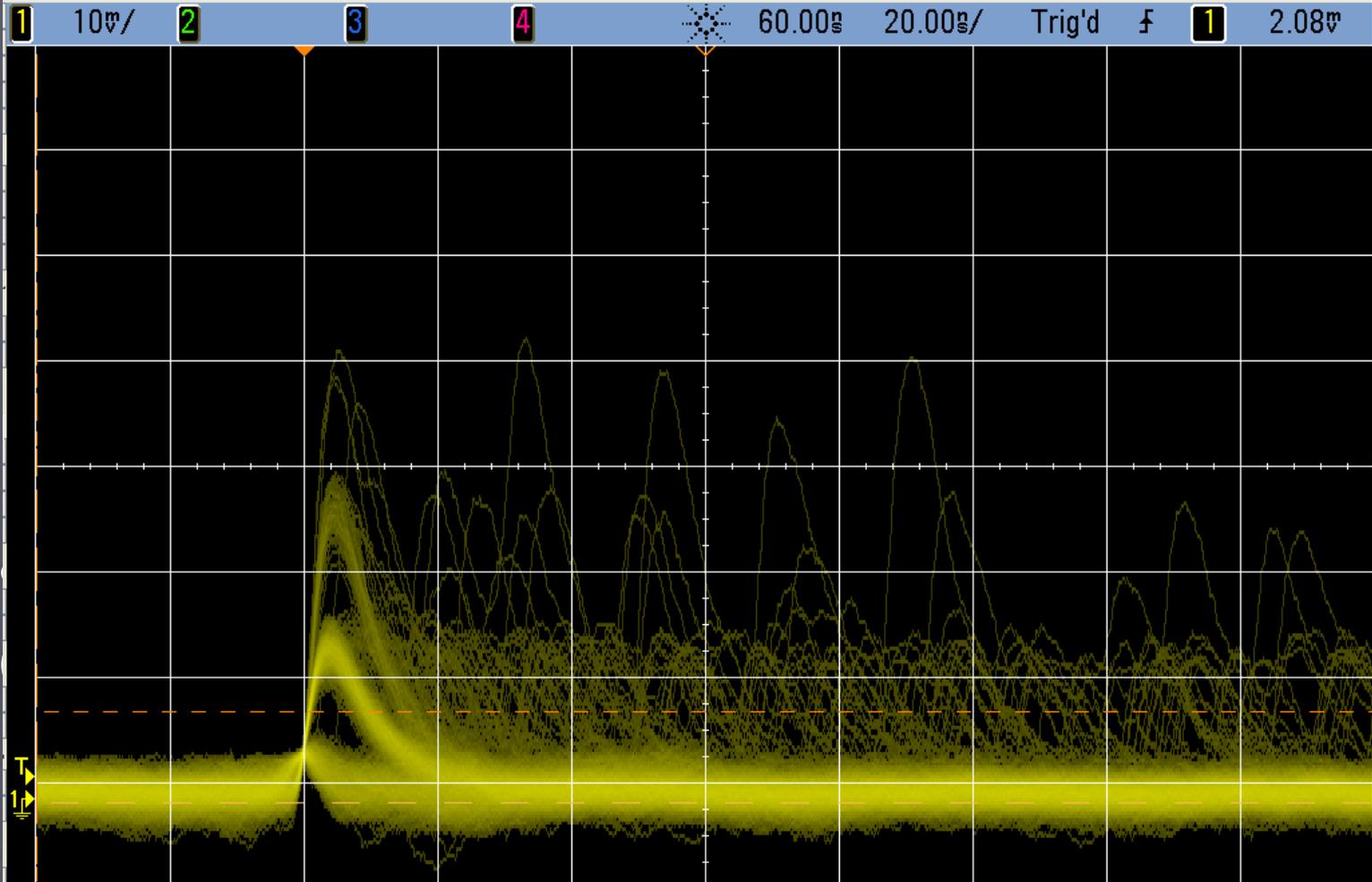
It is that simple

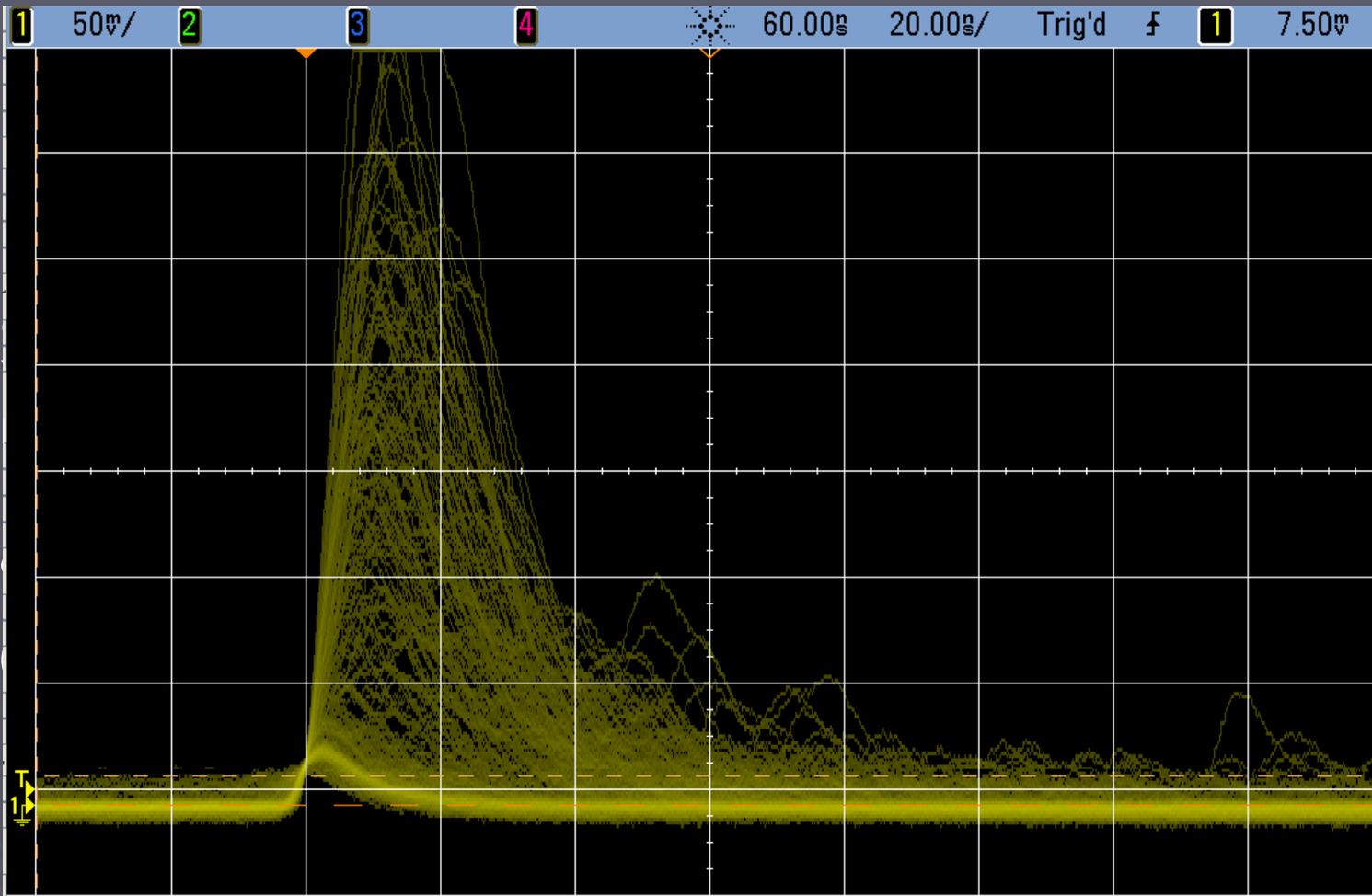
# backup





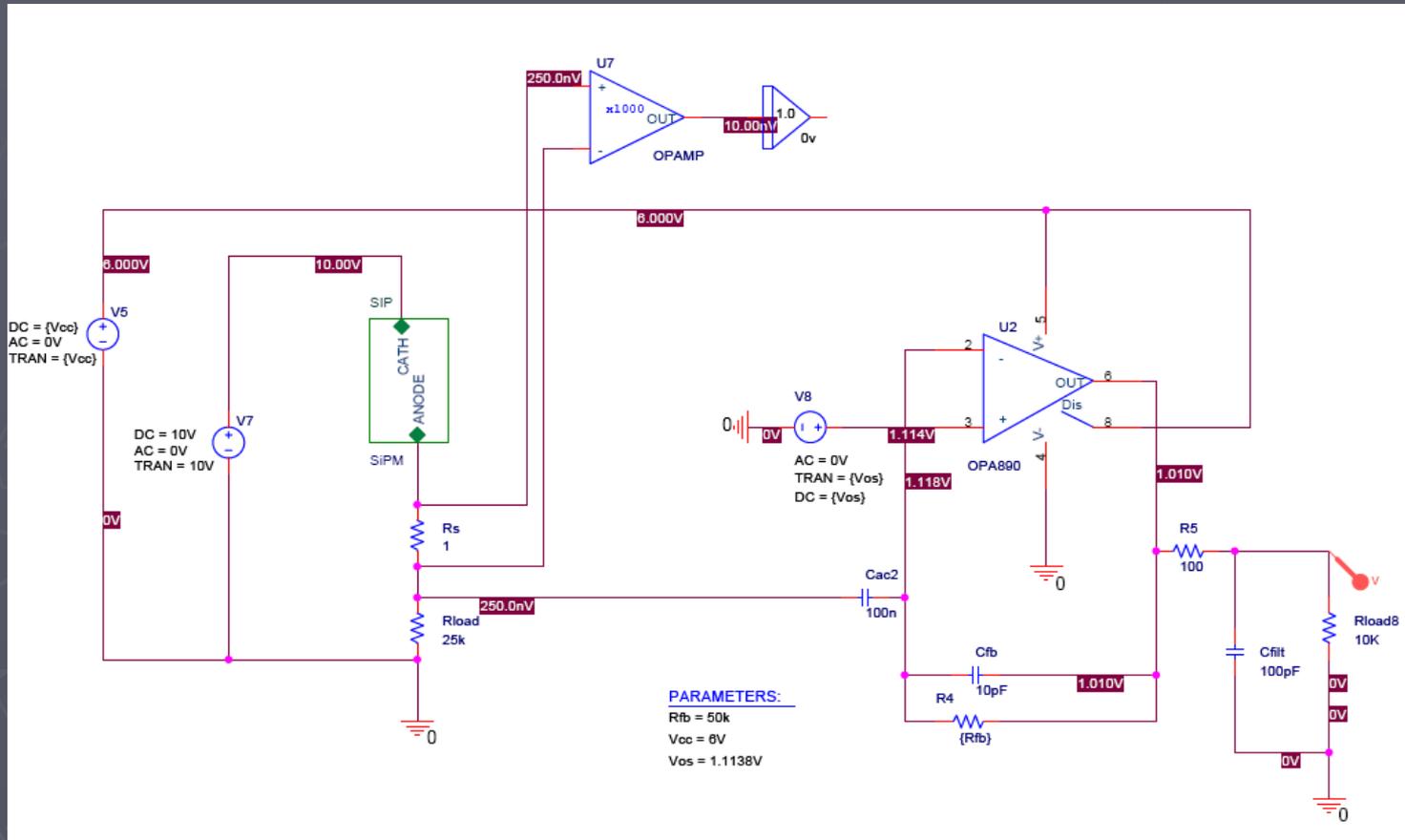
IRST 1.8m with 120Gev Beam at 34V, I=1.1uA





ing  
5C)

# Low power



# Low power



# Proposal

This trace is the simulation of 1pe from an SiPM similar to IRST or MPPC400 at a gain of about 350k

It gives about 5mV output with a decay time of ~1us

Power consumption <10mW

\*\* Profile: "SCHEMATIC1-MPPCsim" [ C:\Projects\ILC\Spice\MPPCsim\_Jan09\mppcsim-pspicefiles\schematic1\mp...  
ate/Time run: 01/22/09 13:53:07 Temperature: 27.0

