TriP Chip
Paul Rubinov, Fermilab

- TriP is the front end preamplifier, trigger and pipeline chip for the VLPC based detectors at Dzero (central fiber tracker and central and forward preshowers)
  - This is an upgrade for an existing system
  - Flaw* in custom chip in original design

- Two main requirements:
  - DO IT FAST
  - DO IT CHEAP
    - Also should work as well as original FE

- Chip design, system design and testing from the experimenters point of view

*Ask me later
The Project

- **People:**
  from Dzero: M. Johnson, F. Borcherding, A. Bross, B. Hoeneisen, J. Estrada, C. Garcia, J. Anderson, P. Rubinov...
  from EED: R. Yarema, A. Mekkaoui, T. Zimmerman, J. Hoff, W. Wester, A. Baumbaugh, K. Knikerbocker, P. Rubinov...

- **The job:**
  Readout signals from the fiber tracker and preshower detectors using VLPCs every 132ns
  Detect hits and send the discriminator bits to trigger system every xing. Store analog info for read out on demand.
The Sensor

- **Visible Light Photon Counters**
  - 100k ch at Dzero
  - 40K gain, 90%QE, 7V bias
  - work at 9K (LHe)

  Two detectors:
  - fiber tracker - 5 to 10 pe
  - preshower - up to 450 pe

**Comments**
- fairly dense
- 6fC/photon typical
- cryostat, long cables

- enormous dynamic range:
  - from 5 to 5000fC

8ch VLPC
hybrid
sitting on a dime
TriP Chip Specs

For Fiber Tracker and Preshower MIP layer (high gain):
- max before saturation = 300 fC
- threshold: 4 to 20 fC
- 99% of channels within ±4 fC
- rms noise < 1.0 fC

For Preshower Detector shower layer (low gain):
- max before saturation = 5000 fC
- typ: 450 photoelectrons = 1890 fC
- threshold desired: 100 to 750 fC

Analog outputs:
- channel uniformity should be within ±3%
- rms noise (high gain) < 1 fC referred to the input
The Problem

- Requirements (cont):
  - Bunch crossing rate = 132 ns
  - Window for charge collection: ... 50 ns ...

Must be able to trig here: i.e. have settled to 1%

Must still be able to collect charge if it comes here

Chip must be FAST
The chip (finally)

Designed by Abder Mekkaoui (J Hoff and T Zimmerman)

1st (and only!) submission

0.25um 2.5V CMOS (TSMC)

4.55mm x 4.80mm

32ch per chip
TriP Chip

- The chip (finally)

Joint submission with SVX4 prototype run (same reticle)

~6800 made

(need ~ 3500 w/spares)

Exactly 1yr from 1st meeting (Jun 2001) with Ray and Abder to chip in hand
TriP Chip

Simplified schematic

Pipeline by T. Zimmerman et. al. also used on SVX4

FrontEnd

ProgInterface

Prog Interface by J. Hoff et. al. also used in FPIX
TriP Chip

The chip (cont.) - front end
TriP Chip

The chip (cont.) - feed back details

![Diagram of the TriP Chip](image)
TriP Chip

The chip (cont.) - feed back details
System Design

- Big advantage - already have system installed
  - Boards exist
  - Testing infrastructure exists

For testing, adapt the TriP to existing boards

Build new MCMs, mount on existing boards - for testing

Full replacement - new boards (200 boards)
System Design

- **System concept critical (for cheap and fast)**
  - Do only what must be done in custom silicon
  - Use commercial chips where possible (ADC, FPGA)
  - Package the chips
Packaging

- **Chip packaging**
  - 124 pins on the die
  - 100 pins on the package
  - Electrical performance in testing so far is no diff. between packaged part and wirebonded bare die

**ASAT ExposedPadPack**
(Other companies have similar technology)
- Large metal pad on which die sits exposed on bottom
- Attached with conductive epoxy: very low L ground
Evaluation

• Made new MCMs compatible with existing system
  - Two versions:
    one with single packaged chip
    one with two wire bonded chips

• Tested extensively on bench (D0Note 4009 and 4076)

• Now started testing with VLPCs
Evaluation

Performance: ADC scan
Evaluation

Performance: DISC scan

2002/12/23 21:30

MCMlib-1-Trip 2 w/33pF VTH=203

ID: 300
Entries: 32
Mean: 13.12
RMS: 0.9922

threshold (fC)

MCMlib-1-Trip 2 w/33pF VTH=203

ID: 400
Entries: 32
Mean: 1.344
RMS: 0.2318

sigma (fC)
Evaluation

Performance: timing scan
Evaluation

- The real test:

- Modified existing board with TriP/MCM
- Real VLPCs, real photons!

TriP on MCM2c

- 8 ch with LED pulser
- 8 ch without pulser

Ped width = 2.6 counts = 1.04fC

Data taken Jun 10, 2003

ADC counts (4mv/count)
Evaluation

- It works!

- Modified existing board with TriP/MCM
- Real VLPCs, real photons!
Evaluation

Spectra from cosmics (summed over ch)

Disc Ratio

Pedestal mean = 44 counts
Cut mean = 69 counts = 6 fC
Cut sigma = 2.3 counts = 0.92 fC
Chip Testing

• Do it fast, do it cheap

Chip testing robot/tester box connected to MCMIIc using ShinEtsu MAF2-8 conductive mat
• **132 packaged chips tested**
  10 chips failed Vdd current test, 2 failed register R/W
  Functional testing of chips underway

• **90% are ok... so far**

![](chart1.png)

Trip Chip Current Measurements (Vdd)

Current slope from DACs R1,R4,R5,R8
## Conclusions

### From Dzero

#### Window for charge collection:
- 40 to 45ns
- Not optimized yet. Probably ok.

#### Digital outputs:
- risetime controlled: no
- active only during reset: no
- No, but work around was found.

#### Threshold setting (high gain):

<table>
<thead>
<tr>
<th>Condition</th>
<th>Result</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>0 to 100fC with 7bit control</td>
<td>satisfied (prelim)</td>
<td>More testing, especially with larger inj charges would be useful.</td>
</tr>
<tr>
<td>99% of channels within 4fC</td>
<td>4fC w/o caps</td>
<td>Packaged part, no load.</td>
</tr>
<tr>
<td></td>
<td>5fC w/33pF</td>
<td></td>
</tr>
<tr>
<td></td>
<td>acceptable</td>
<td></td>
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<td>rms noise &lt;1fC</td>
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<td></td>
<td>&lt;1fC w/o caps</td>
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<td></td>
<td>1.3fC w/33pF</td>
<td>33pF load.</td>
</tr>
<tr>
<td></td>
<td>acceptable</td>
<td></td>
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<tr>
<td>Threshold setting (low gain)</td>
<td>not yet tested</td>
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#### Analog outputs:

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<tr>
<td>16:1 analog mux at 7.6MHz</td>
<td>satisfied</td>
<td>Packaged part, no load.</td>
</tr>
<tr>
<td>ch to ch uniformity within ±3%</td>
<td>6% slope, 3% peds</td>
<td>33pF load.</td>
</tr>
<tr>
<td></td>
<td>8% slope, 5% peds</td>
<td>Some spread is due to layout of MCM.</td>
</tr>
<tr>
<td></td>
<td>satisfied</td>
<td>Packaged part, no load.</td>
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<tr>
<td>rms noise &lt;1fC</td>
<td>0.6fC RMS w/o C</td>
<td></td>
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<td></td>
<td>satisfied</td>
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</tr>
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<td></td>
<td>1.2fC RMS w/ 33pF</td>
<td></td>
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<td>acceptable</td>
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Conclusions

- Chip worked on the first try.
- It's not perfect but it is, in our judgment, good enough.
- We want to continue development because the requirements have changed*.

*Ask me later if you are interested in an energetic discussion of accelerator physics.

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<td>2pF charged with 1s</td>
<td>4pF w/o caps</td>
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<td>5fC w/33pF</td>
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From Dzero note 4076
Evaluation

Performance (from Dzero Note 4076)